論理回路

3年生産システム工学科(情報コース)

実施時期 2020/10-2021/2

基本的な論理素子の動作を理解する。

この実験には

- 「ディジタル回路(コロナ社)」(教科書)
- ペン(色は黒) (鉛筆不可)
- ノートまたはレポート用紙

が必要です。
修正テープ(修正ペン・修正液等)を使用した提出物は受理しないので注意すること。
必須ではないがつぎのものを用意することを推奨する。

- スマートフォンまたはタブレット(学内LANを使用せず、通信会社によるデータ通信ができるもの)
- 方眼紙
- 赤ペン,青ペン　または　蛍光ペン

論理回路(3SJ)　※本日実験終了時に提出　修正テープ(修正ペン・修正液等)の使用は認めない

実験日　　/　　出席番号　　氏名

LED 点灯時を 1,LED 消灯時を 0 とする

NOT ゲート(74LS04)

入力 A	出力 Y
0	
1	

AND ゲート(74LS08)

入力 A	入力 B	出力 Y
0	0	
0	1	
1	0	
1	1	

OR ゲート(74LS32)

入力 A	入力 B	出力 Y
0	0	
0	1	
1	0	
1	1	

XOR ゲート(74LS86)

入力 A	入力 B	出力 Y
0	0	
0	1	
1	0	
1	1	

NAND ゲート(74LS00)

入力 A	入力 B	出力 Y
0	0	
0	1	
1	0	
1	1	

NOR ゲート(74LS02) ピン配置に注意

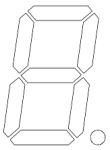
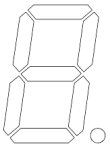
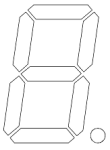
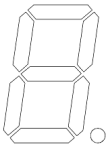
入力 A	入力 B	出力 Y
0	0	
0	1	
1	0	
1	1	

この実験からわかること

論理回路(3SJ)　※本日実験終了時に提出　修正テープ(修正ペン・修正液等)の使用は認めない

実験日　　/　　出席番号　　氏名

選んだLED:　　(Anode Cathode common)

入力		LED	出力(LED制御線)							memo
x (D9)	y (D8)		a	b	c	d	e	f	g	
0	0									
0	1									
1	0									
1	1									

論理式と回路図

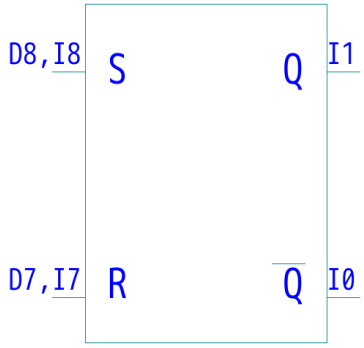
動作 確認　　印

論理回路3(3SJ)　※本日実験終了時に提出

実験日　　/　　出席番号　　氏名

つぎの論理回路・論理素子について、$Q\overline{Q}$を観測し、記録しなさい。
回路図には端子名($Q\overline{Q}$)、素子名、ピン番号を明記する。

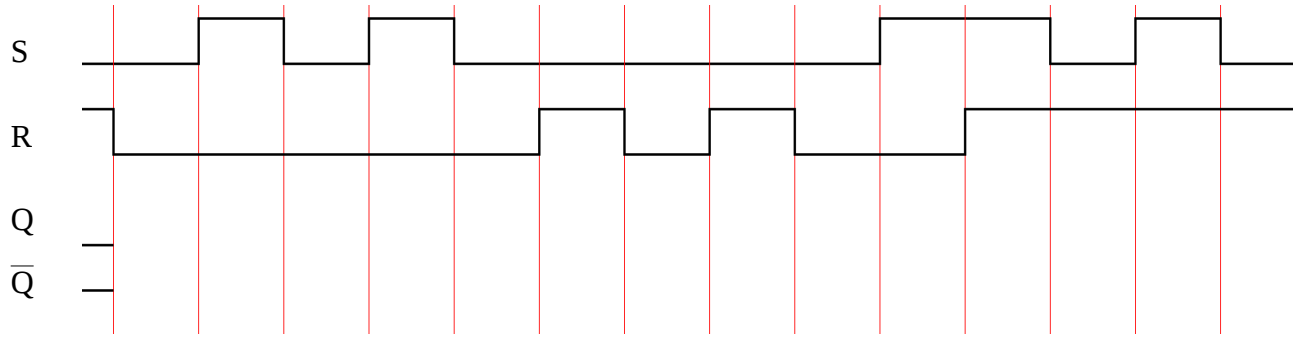
1 RS-Latch(RS-FF)



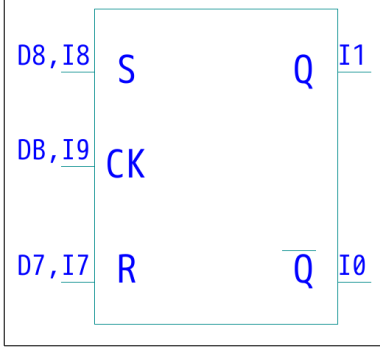
[回路図]　NOR ゲート 2 個で RS-Latch(RS-FF)をつくる

S(D8,I8)

R(D7,I7)



2 ポジティブレベルトリガ RS-Latch(RS-FF)

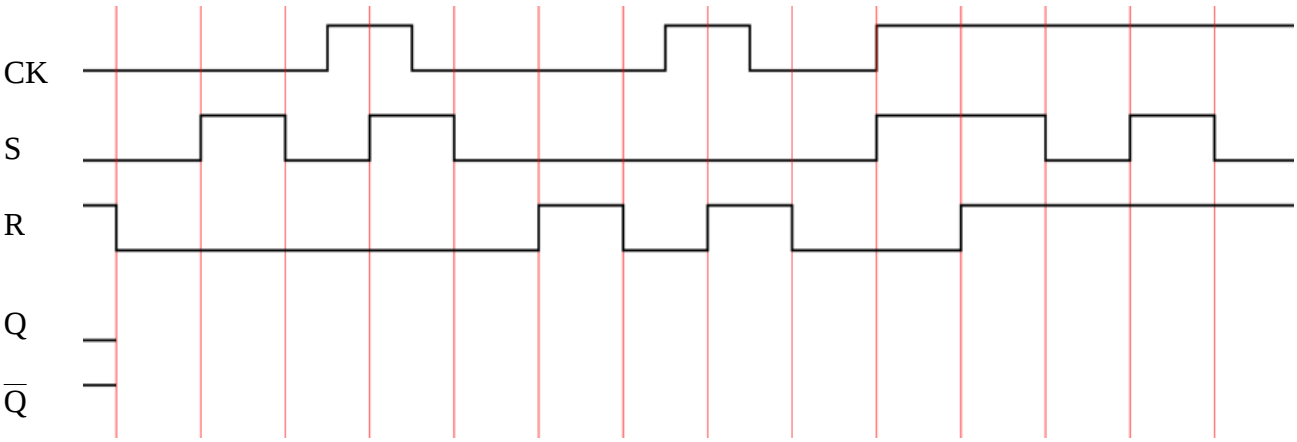


[回路図]　1.RS-Latch(RS-FF)に AND ゲート 2 個を追加する

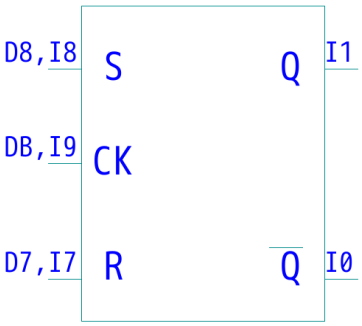
S(D8,I8)

CK(DB,I9)

R(D7,I7)



3 R優先RS-Latch(RS-FF)

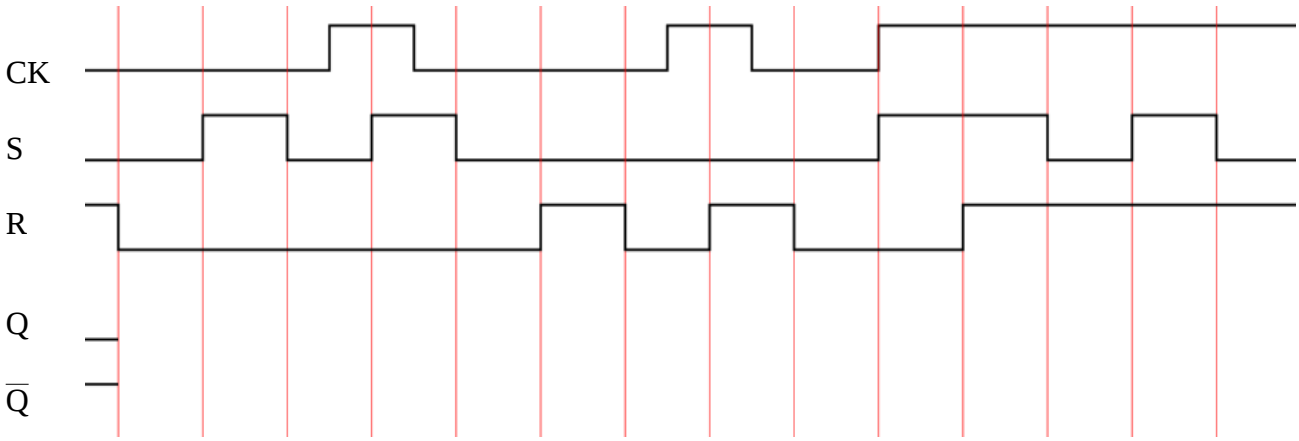


[回路図]　2 ポジティブレベルトリガRS-Latch(RS-FF)に未使用のNORゲートをNOTゲートとして追加する

S(D8,I8)

CK(DB,I9)

R(D7,I7)

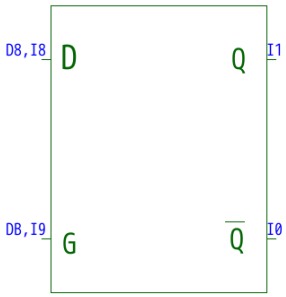


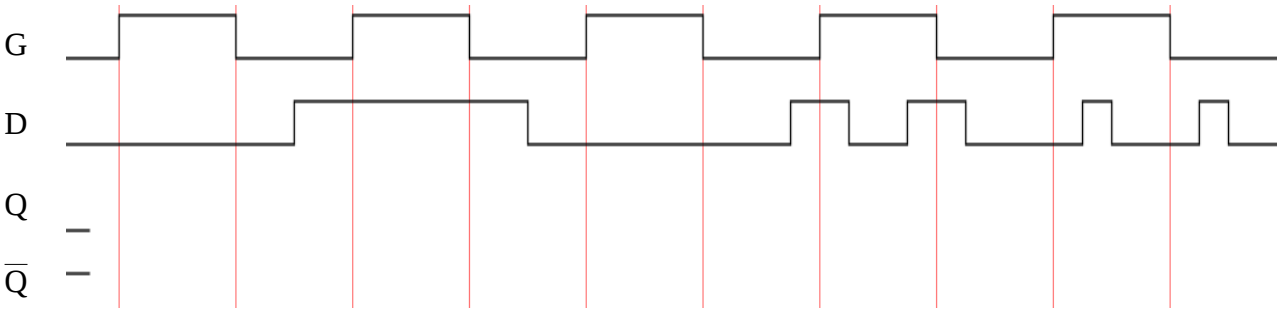
論理回路2(3SJ)　※本日実験終了時に提出

実験日　　/　　出席番号　　氏名

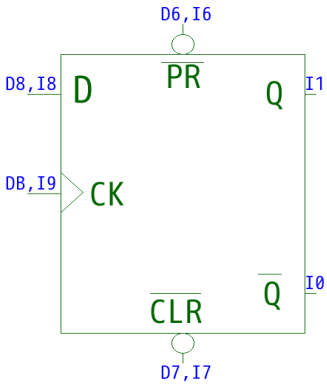
つぎの論理素子について、Q,$\overline{Q}$を観測し、記録しなさい。Qの初期値は0とする。

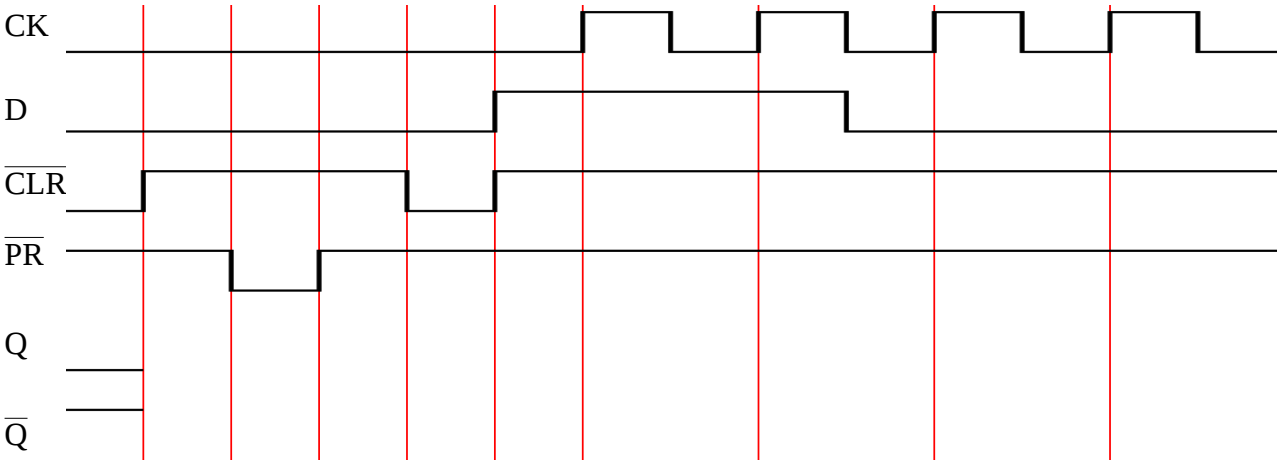
1 D-Latch(74LS75)　ピン番号を記入する。
　ゲートGをクロックCKとして使用する。





2 D-FF(74LS74) ピン番号を記入する。



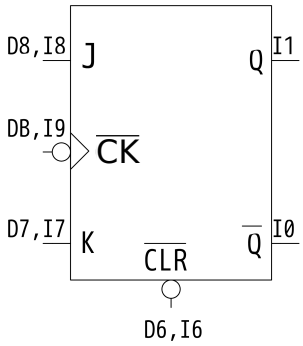


論理回路(3SJ)　※本日実験終了時に提出

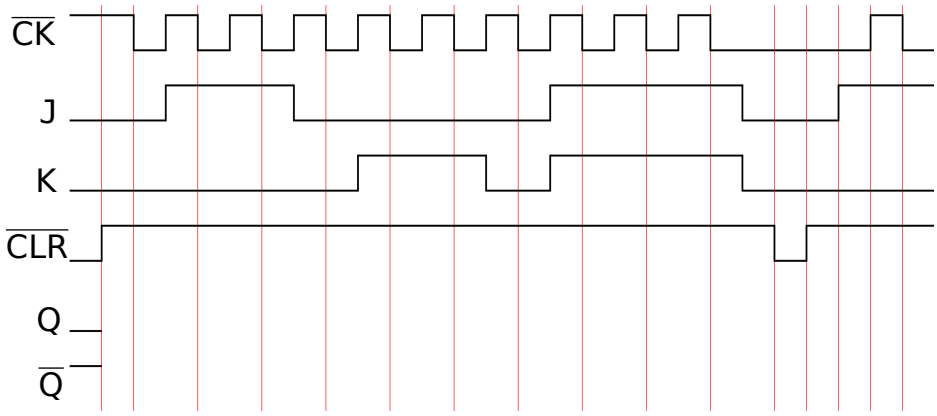
実験日　　/　　出席番号　　氏名

タイミングチャート中の Q,$\overline{Q}$,QB,QC,QD を観測し記録する。

1 JK-FF



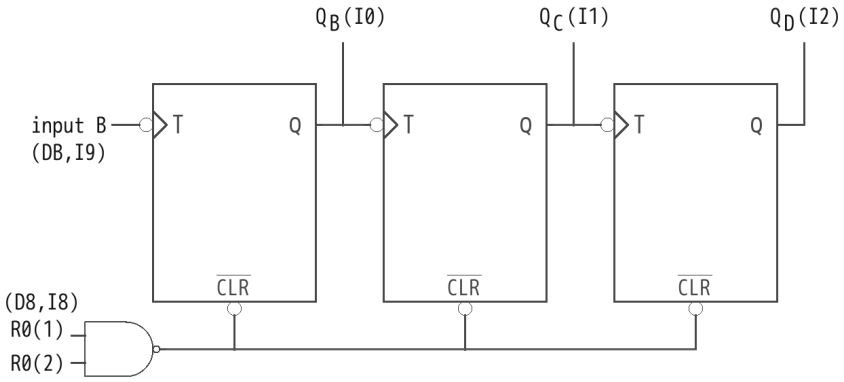
74LS73



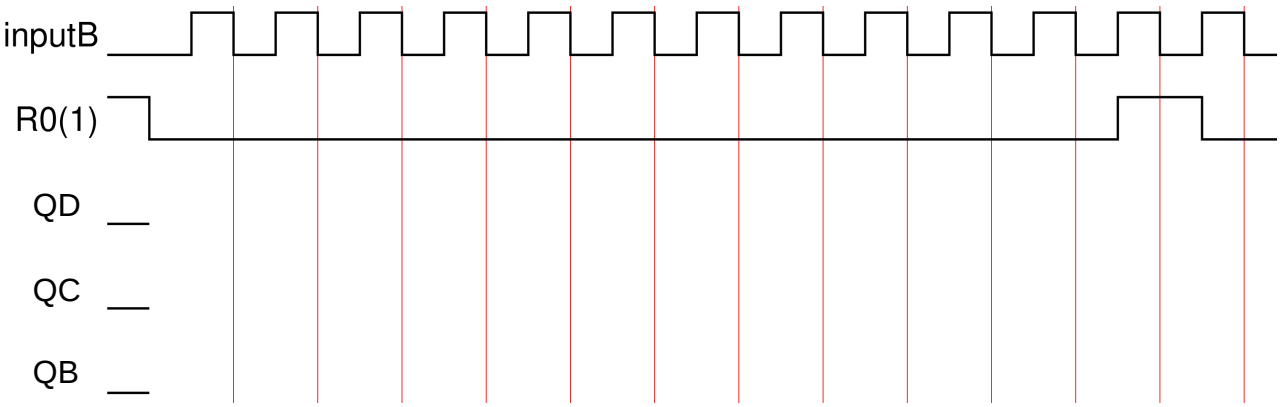
2 非同期 3 ビットカウンタ(リップルカウンタ)

[注意事項]

常に
　input A="0"(GND)
　R0(2)="1"(Vcc)
　Q_A=開放
とする。



74LS93



論理回路(3SJ)　※本日実験終了時に提出

実験日　/　　出席番号　　氏名

1.目的

論理回路(3 年生)に基づき、順序論理回路(同期カウンタ)を作り、動作を確認する。

2.実験手順

(1)状態遷移図　　必要に応じて状態遷移表やタイミングチャートを作る。
(2)遷移条件決定　　(1)に基づき、JK 等の入力条件を決定する。(応用方程式または励起表を使う。)
(3)動作確認(机上)　(2)に基づき、カウンタの動作を検討する。異常シーケンスが発生しないことも確認する。
(4)論理回路図設計　論理 IC の選択とパッケージ内素子の結線を決定し、回路図を描く。
(5)動作確認(実回路)　(4)に基づき、カウンタを作り、動作を確認する。

3.仕様

(1)カウンタの動作は当日指定する。状態遷移図を描画する。
(2)JK-FF(74LS73)を使用する。必要に応じて AND ゲート等を使用してよい。
(3)$\overline{\text{CLR}}$ をアクティブにするとカウンタは S0 に初期化する。$\overline{\text{CLR}}$ はトグルスイッチ SW9(D9)を使用する。
(4)クロックは PSW2(DB)を使用し、プッシュスイッチで手動入力する。
(5)出力は LED3,2,1,0(I3,I2,I1,I0)を使用する。LED0 を LSB とする。

4.実験結果

実験結果はレポート用紙(A4 版)に記載する。レポート用紙は左側 2cm を余白とする。
論理回路図が正しく、かつ、設計とおりに動作したことを確認した後、実験結果を提出する。

5.追加事項

実験が終了しない場合、「追加事項」を実験結果に追記する。追加事項が納得できるものである場合のみ、後日実験を行うことができる。
(1)カウンタの設計・動作確認が完了しない場合、その原因を説明しなさい。
実験内容から見て「時間が足りない。」「論理回路を理解していない。」は理由として認めない。
(2)実回路が正常に動作しない場合、その原因を説明しなさい。
「設計が間違っていた。」「回路の結線が間違っていた。」は理由として認めない。

状態遷移図

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS00
Quad 2-Input NAND Gate

General Description

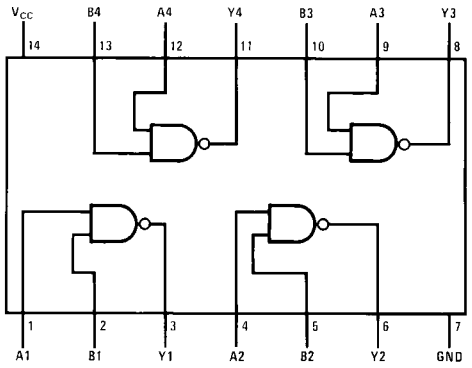
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.4	4.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

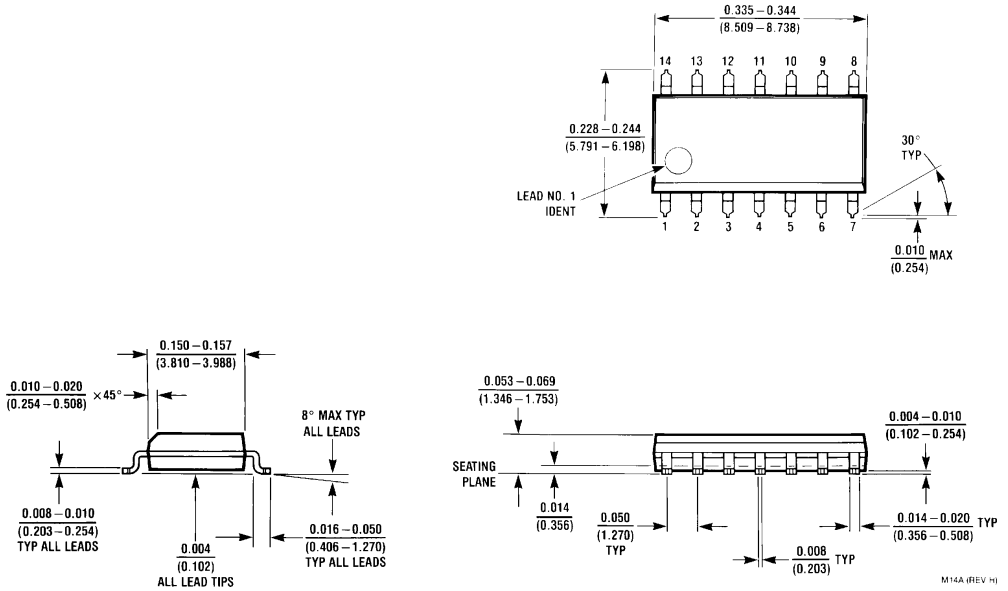
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

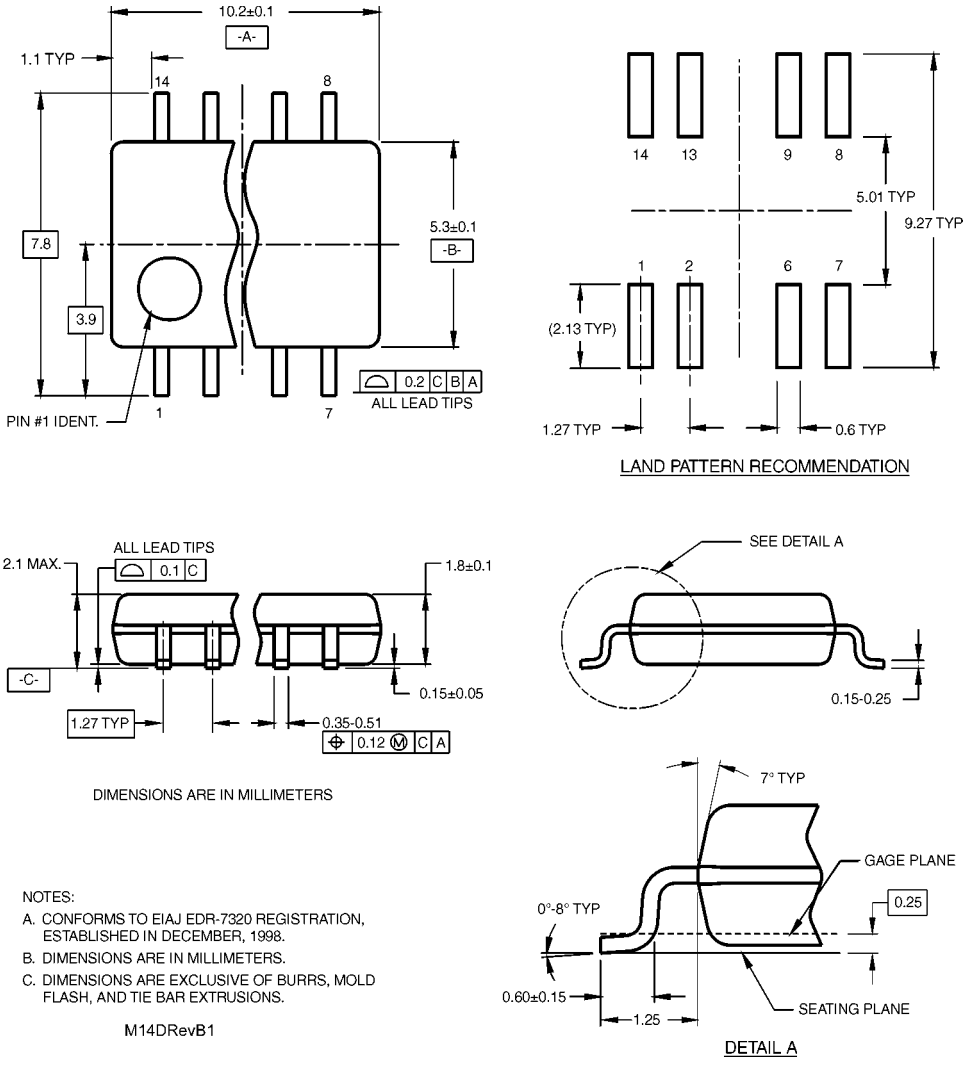
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

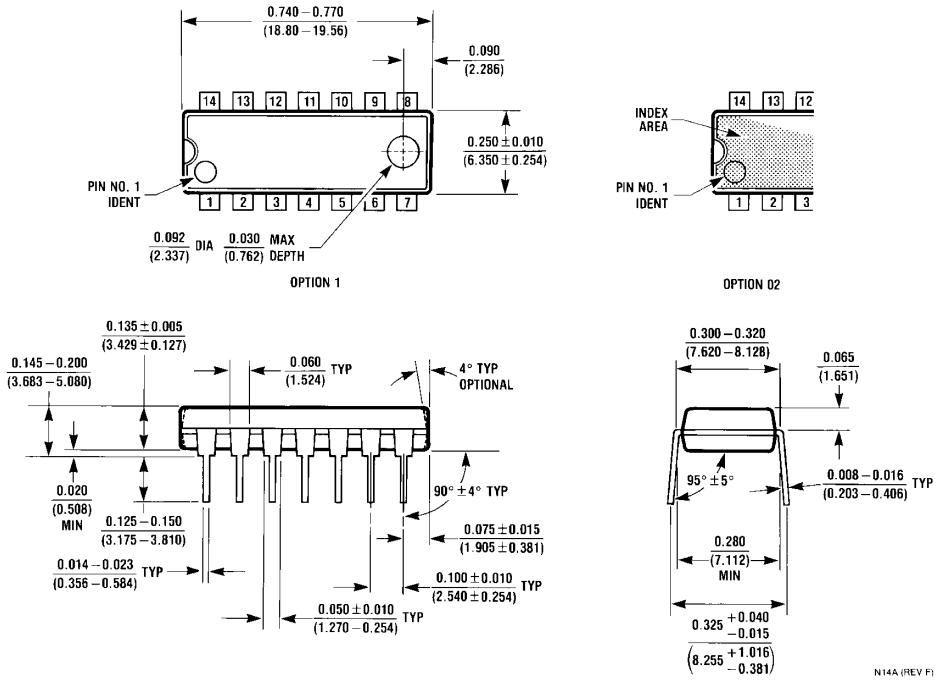
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

FAIRCHILD SEMICONDUCTOR™

May 1986
Revised March 2000

DM74LS02
Quad 2-Input NOR Gate

General Description

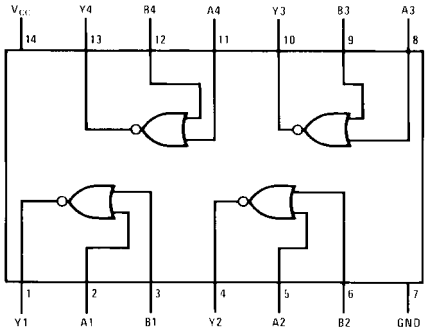
This device contains four independent gates each of which performs the logic NOR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS02M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS02N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.40	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.6	3.2	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.8	5.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

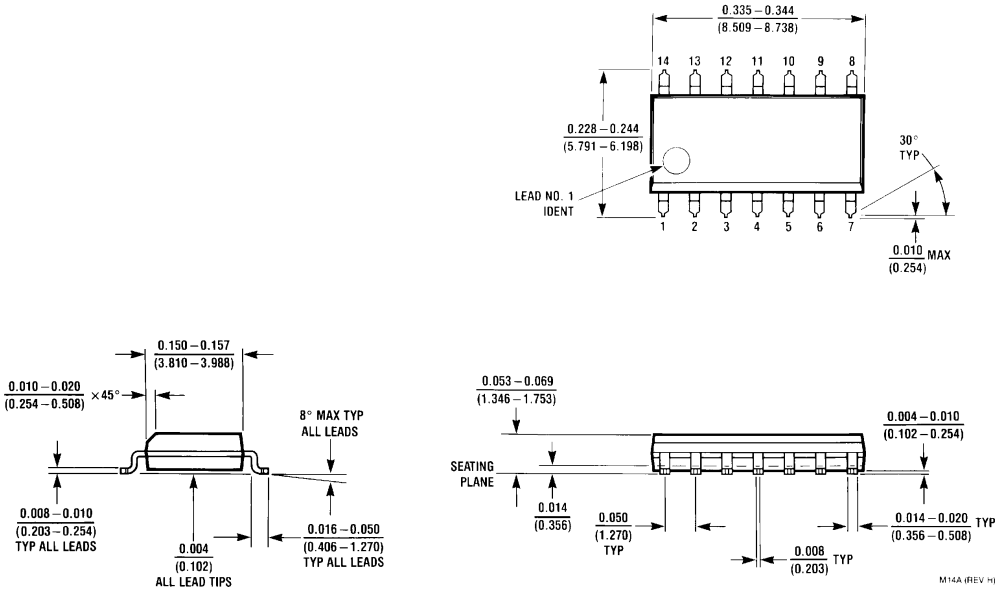
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

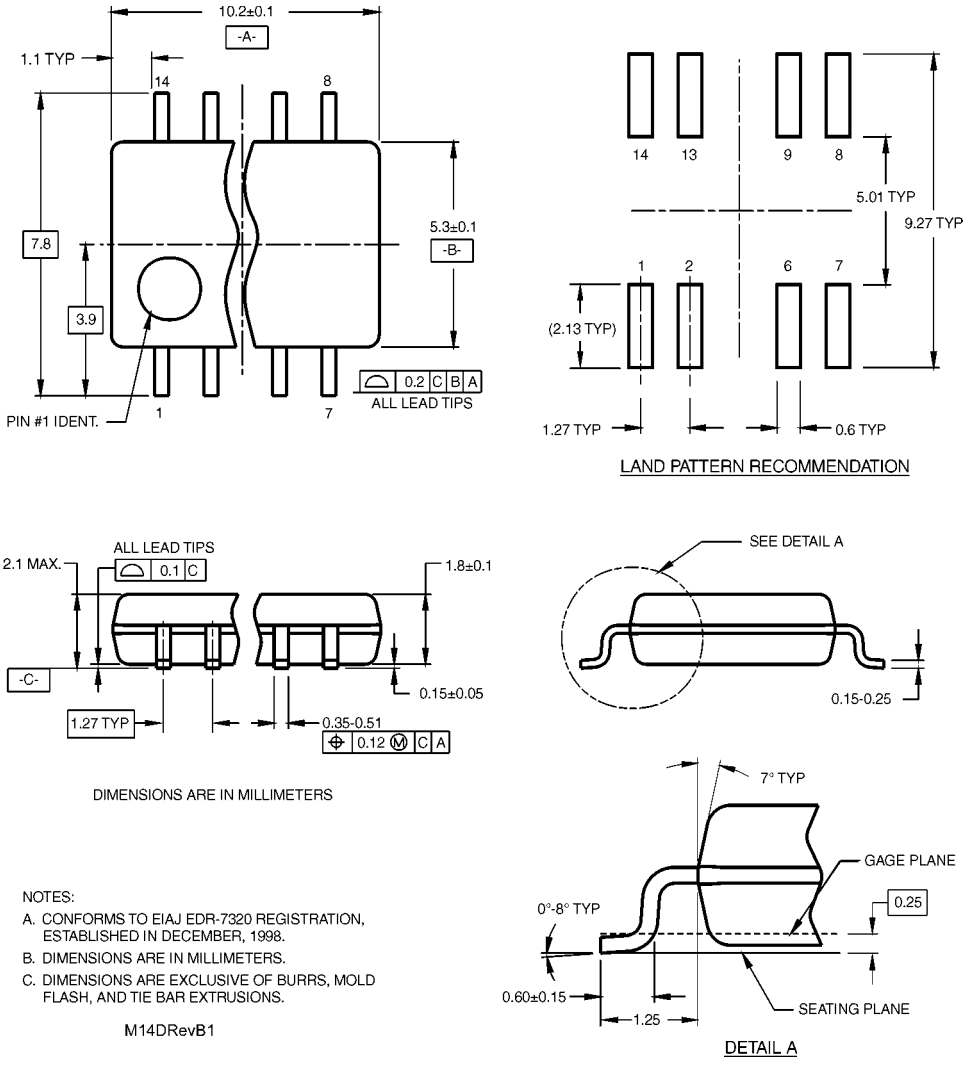
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		13		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		10		15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

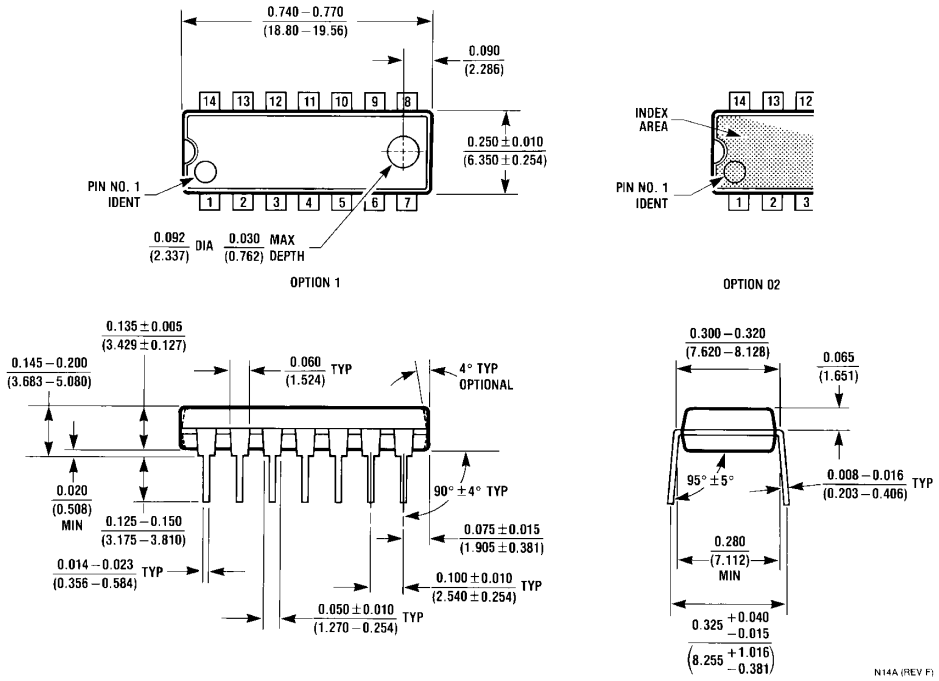
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS04
Hex Inverting Gates

General Description

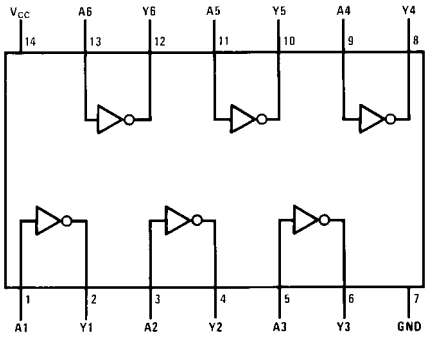
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.2	2.4	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		3.6	6.6	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

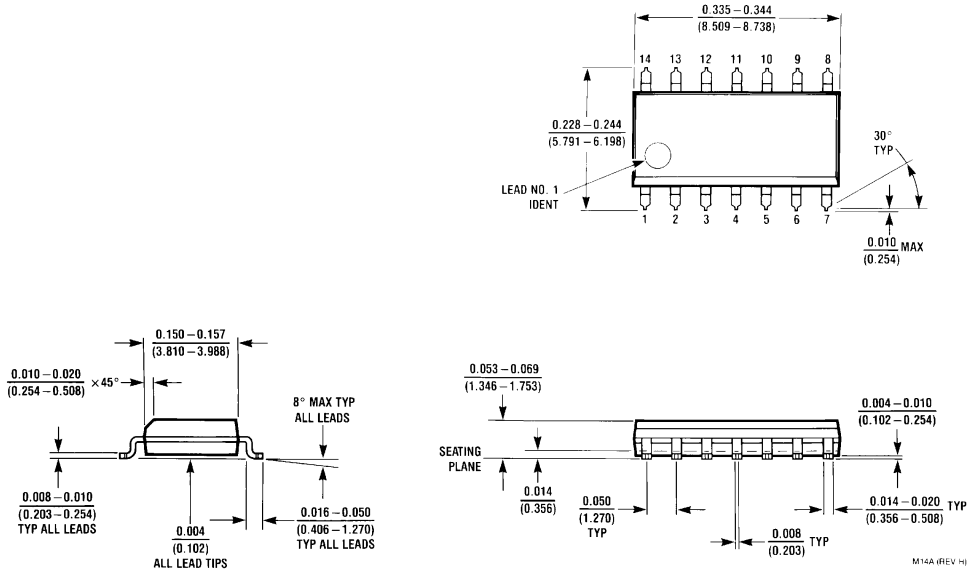
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

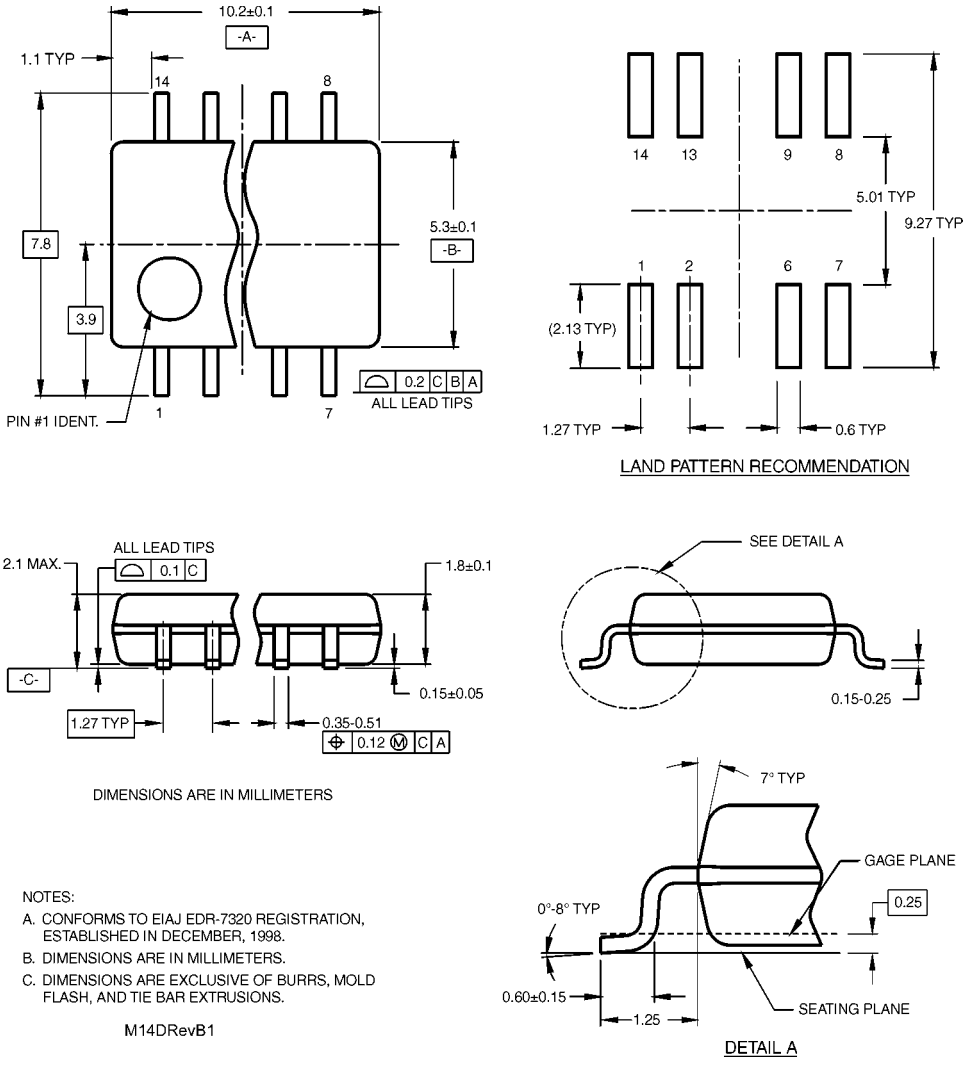
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

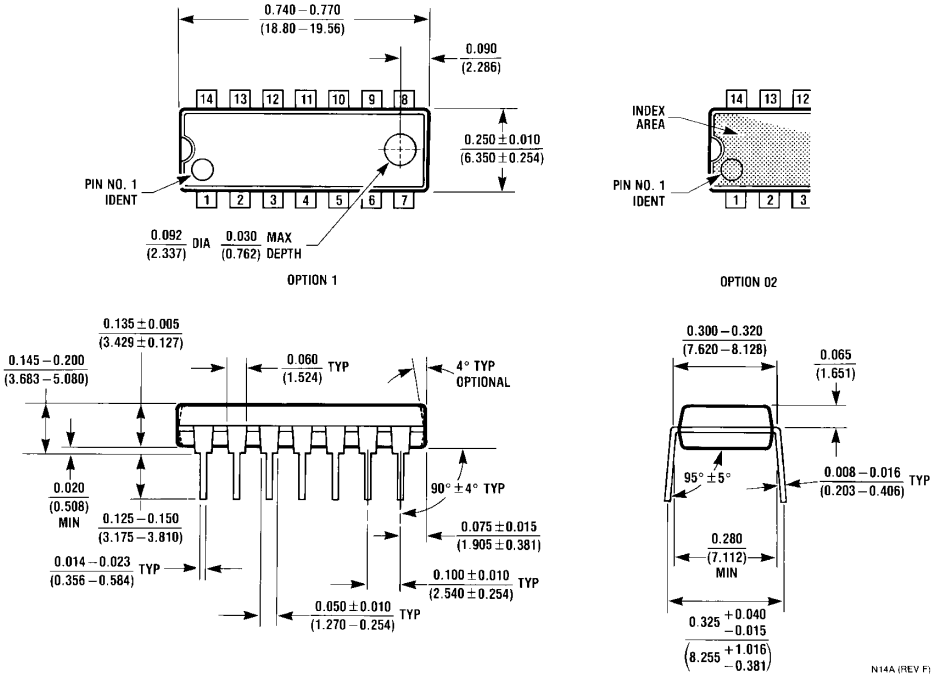
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS08
Quad 2-Input AND Gates

General Description

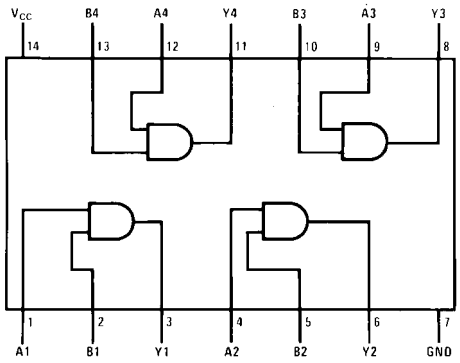
This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		2.4	4.8	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		4.4	8.8	mA

Switching Characteristics

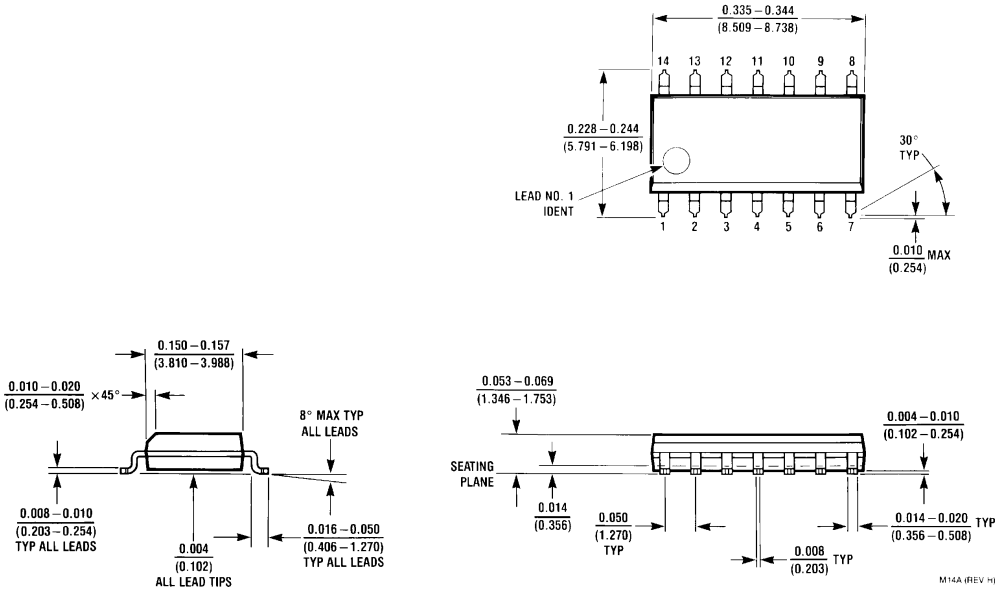
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

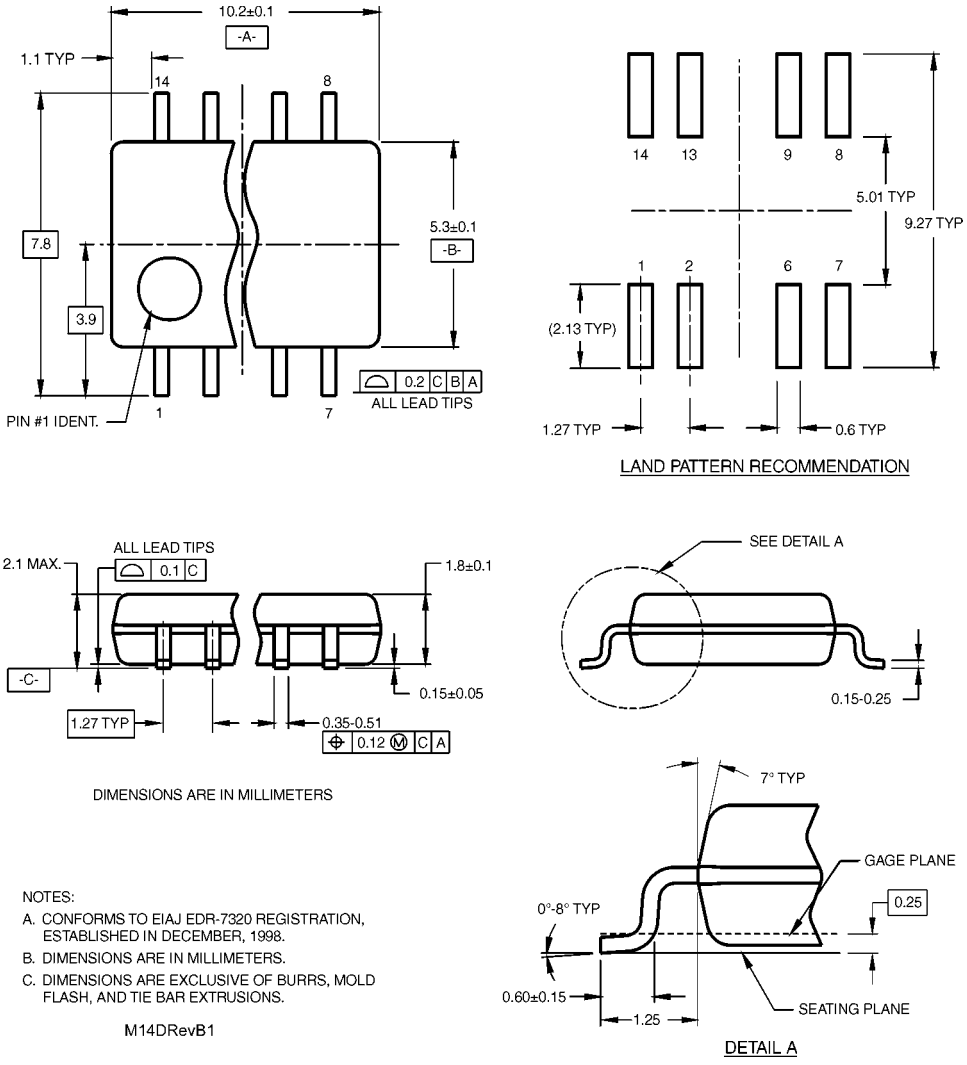
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

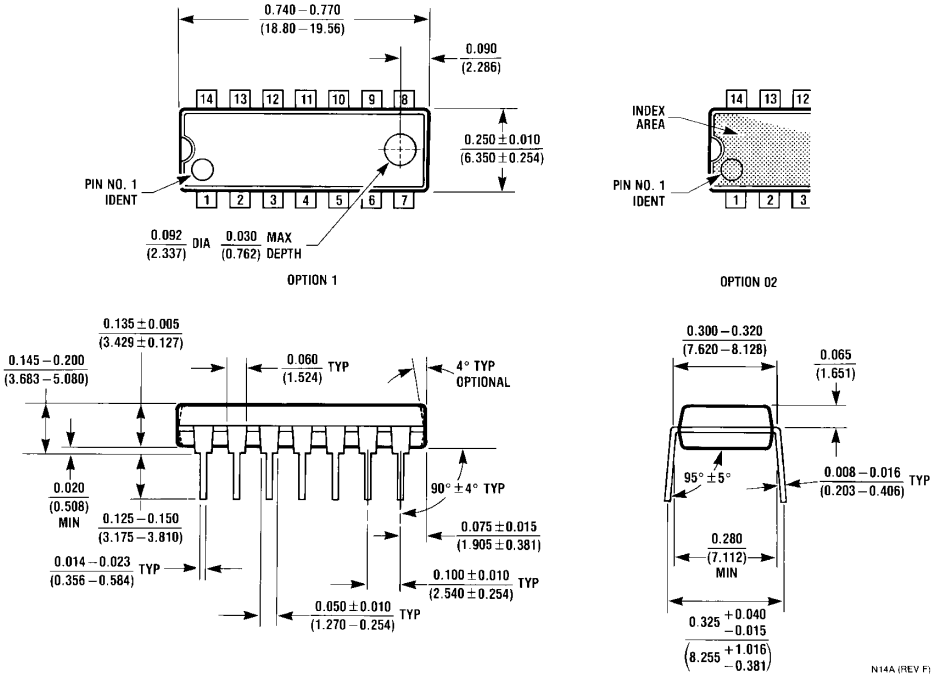
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS10
Triple 3-Input NAND Gate

General Description

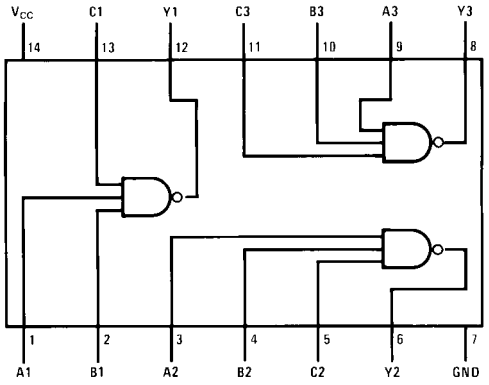
This device contains three independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS10M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS10N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		0.6	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		1.8	3.3	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

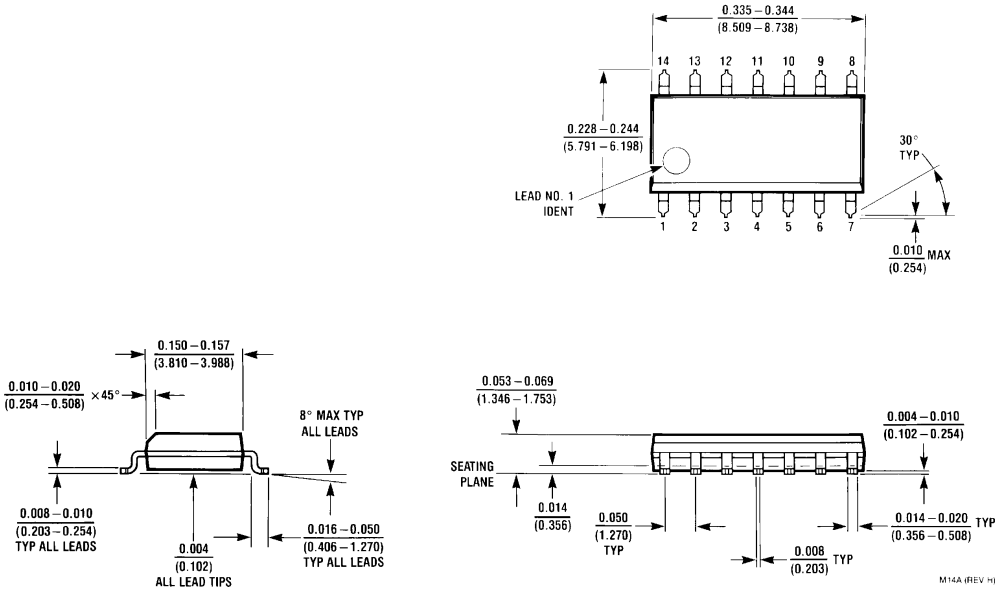
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

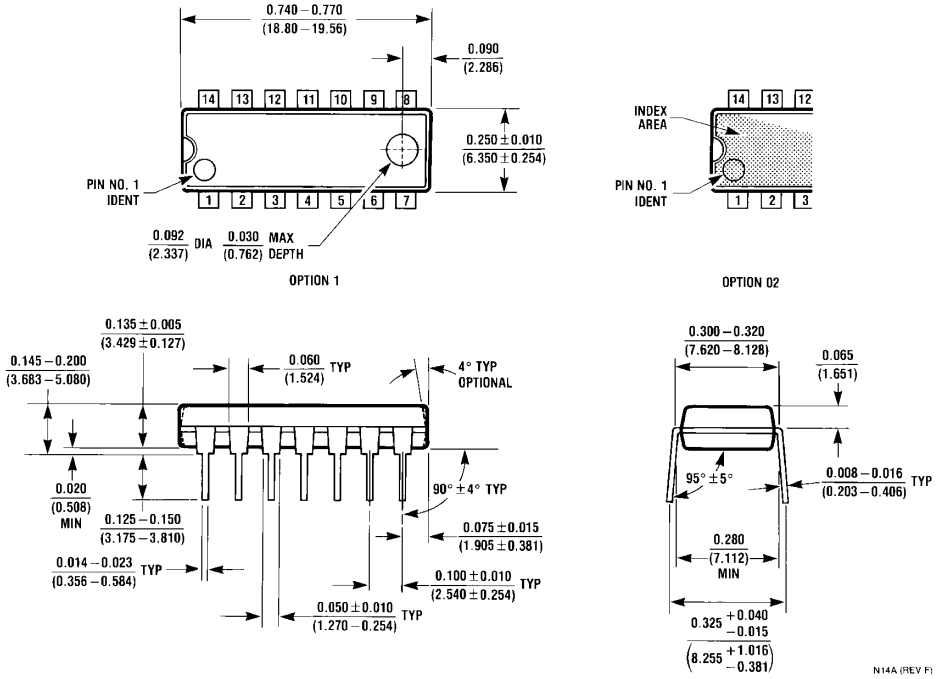
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

HD74LS32

Quadruple 2-input Positive OR Gate

REJ03D0405–0200
Rev.2.00
Feb.18.2005

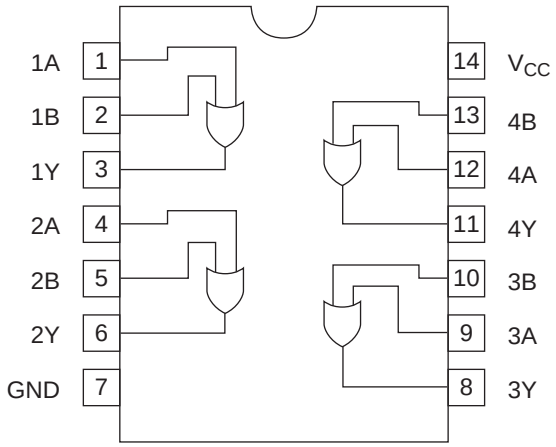
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS32P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS32FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

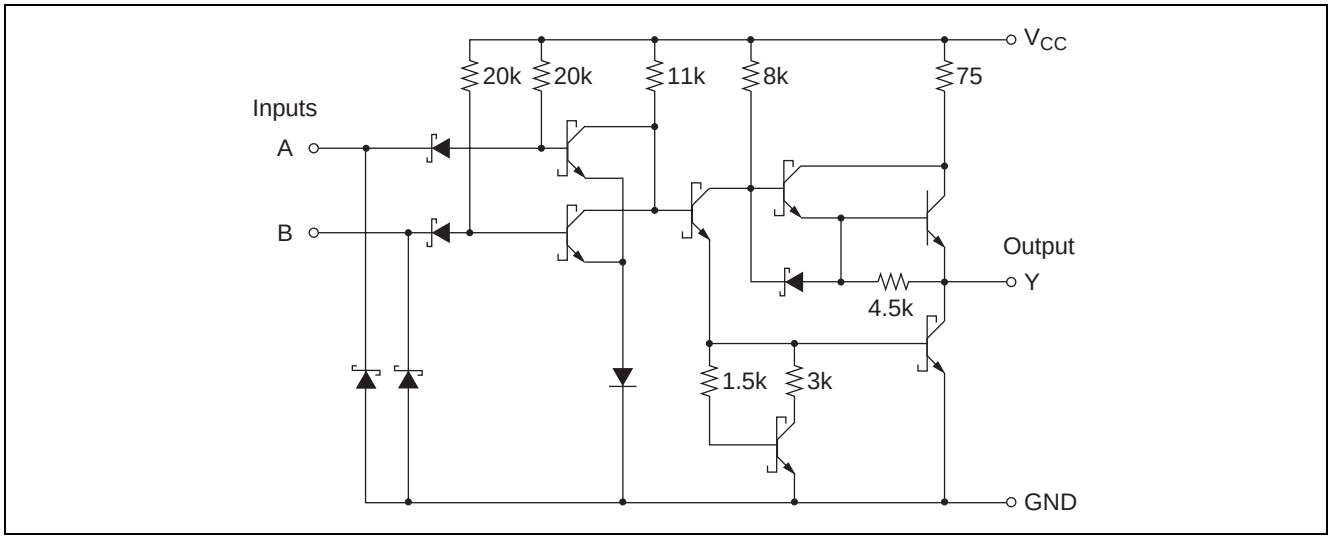
Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Circuit Schematic (1/4)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IL} = 0.8 V
		—	—	0.4		I_{OL} = 4 mA, V_{CC} = 4.75 V, V_{IL} = 0.8 V
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current	I_{CCH}	—	3.1	6.2	mA	V_{CC} = 5.25 V
	I_{CCL}	—	4.9	9.8	mA	V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Note: * V_{CC} = 5 V, Ta = 25°C

Switching Characteristics

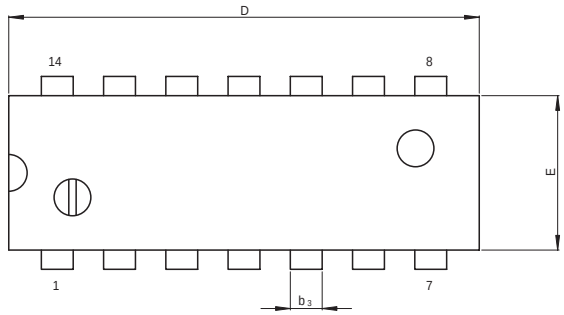
(V_{CC} = 5 V, Ta = 25°C)

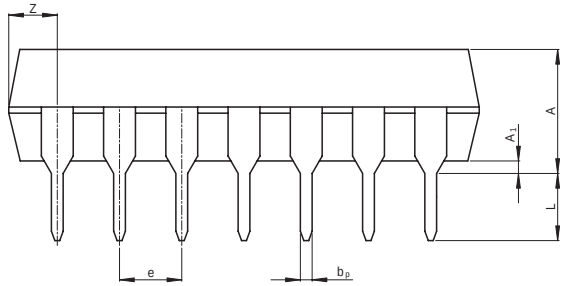
Item	Symbol	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	—	14	22	ns	C_L = 15 pF, R_L = 2 kΩ
	t_{PHL}	—	14	22	ns	C_L = 15 pF, R_L = 2 kΩ

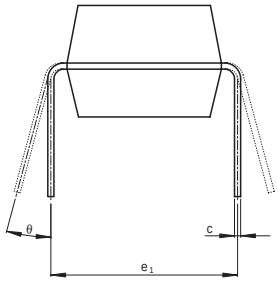
Note: Refer to Test Circuit and Waveform of the Common Item "TTL Common Matter (Document No.: REJ27D0005-0100)".

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-B	DP-14AV	0.97g



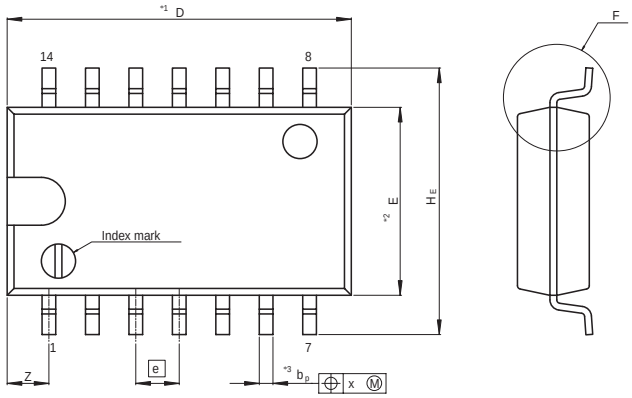




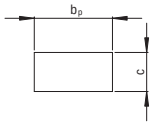
(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A_1	0.51	——	——
b_p	0.40	0.48	0.56
b_3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	2.39
L	2.54	——	——

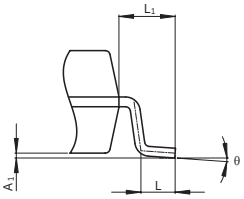
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	1.42
L	0.50	0.70	0.90
L_1	——	1.15	——

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Colophon .2.0

HD74LS73A

Dual J-K Flip-Flops (with Clear)

REJ03D0414–0300
Rev.3.00
Jul.22.2005

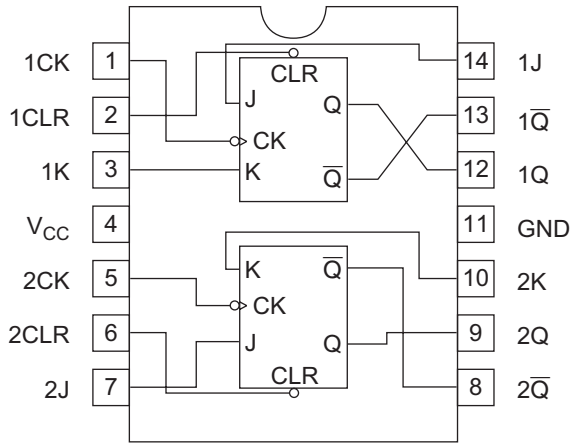
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS73AP	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS73ARPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



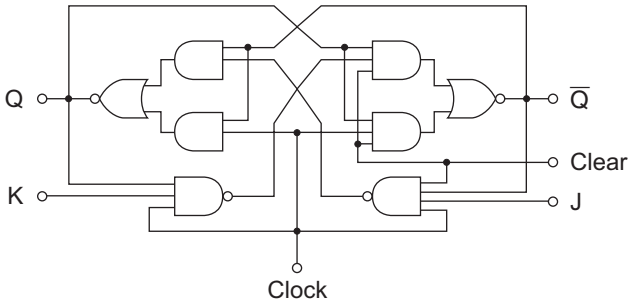
(Top view)

Function Table

Inputs				Outputs	
Clear	**Clock**	**J**	**K**	**Q**	**$\overline{Q}$**
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_O	$\overline{Q}_O$

H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,
Q_0; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of $\overline{Q}_0$ or level of Q before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	$t_{w\ (Clock\ High)}$	20	—	—	ns
	$t_{w\ (Clear\ Low)}$	25	—	—	
Setup time	$t_{su\ (“H”\ Data)}$	20↓	—	—	ns
	$t_{su\ (“L”\ Data)}$	20↓	—	—	
Hold time	t_h	0↓	—	—	ns

Note: ↓; The arrow indicates the falling edge.

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
		V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.4		I_{OL} = 4 mA
Input current	J, K	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	Clear		—	—	60		
	Clock		—	—	80		
	J, K	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Clear		—	—	–0.8		
	Clock		—	—	–0.8		
	J, K	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Clear		—	—	0.3		
	Clock		—	—	0.4		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**		I_{CC}	—	4	6	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

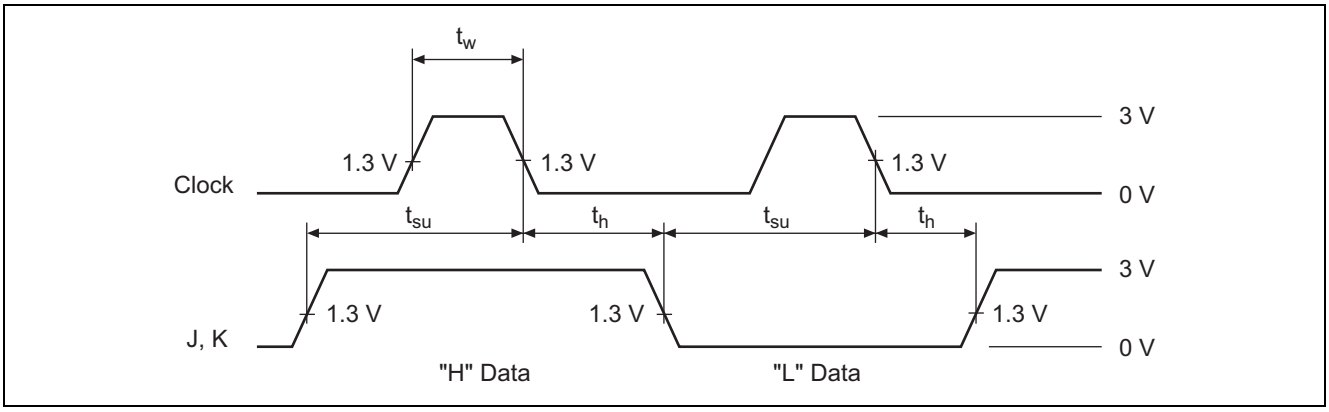
** With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At time of measurement, the clock input is founded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			30	45	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clear Clock	Q, $\overline{Q}$	—	15	20	ns	
	t_{PHL}			—	15	20	ns	

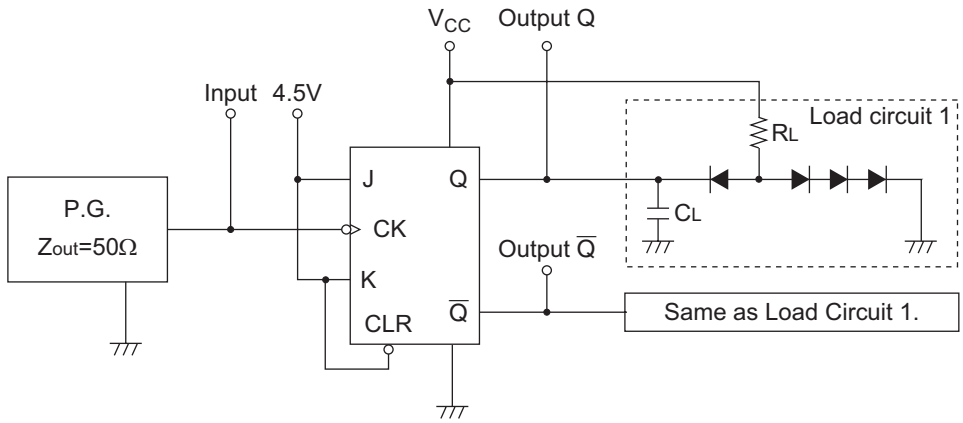
Timing Definition



Testing Method

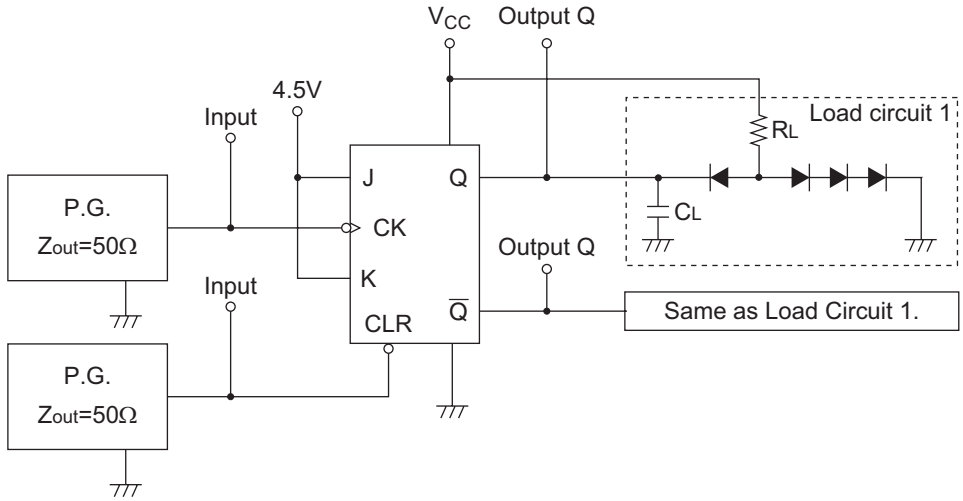
Test Circuit

1. f_{max}, t_{PLH}, t_{PHL}, (Clock→Q, $\overline{Q}$)



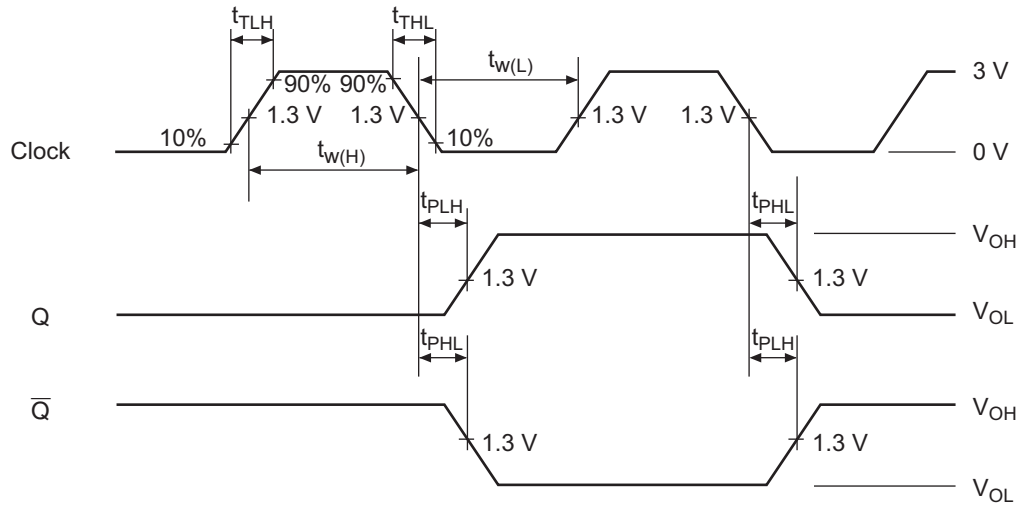
Notes:
1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

2. t_{PHL} (Clear→Q), t_{PLH} (Clear→$\overline{Q}$)



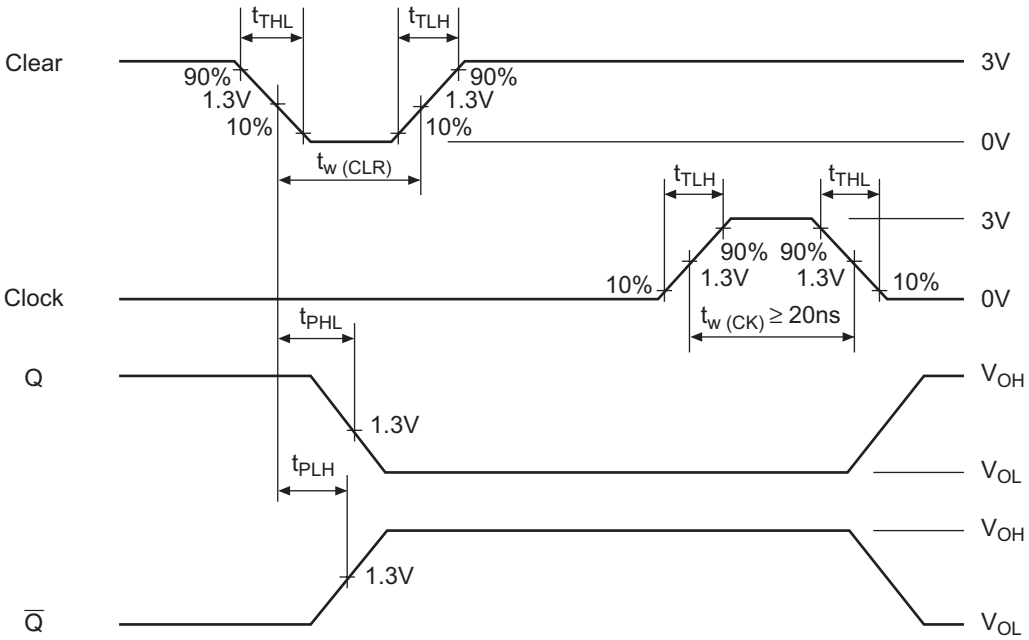
Notes:
1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

Waveforms 1



Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and for f_{max}, $t_{TLH} = t_{THL} \leq 2.5$ ns

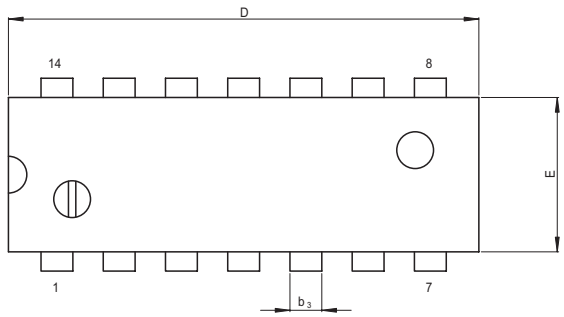
Waveforms 2

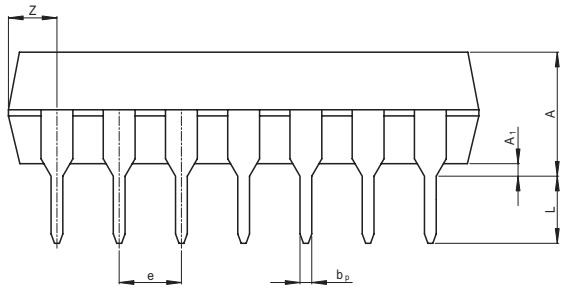


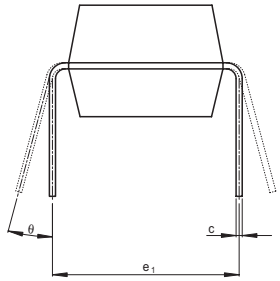
Note: Crear and clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz,

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-B	DP-14AV	0.97g



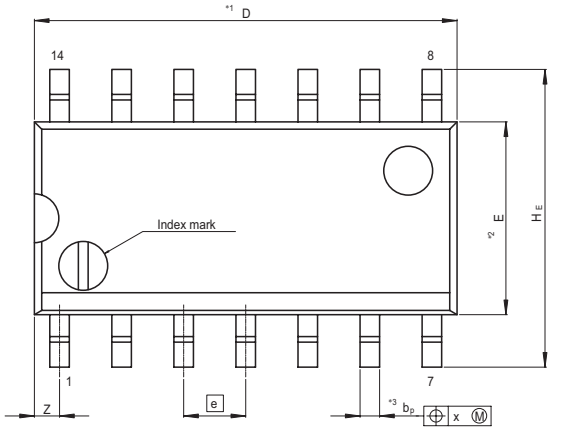


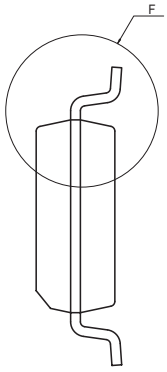


(Ni/Pd/Au plating)

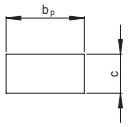
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	2.39
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-3.95x8.65-1.27	PRSP0014DE-A	FP-14DNV	0.13g

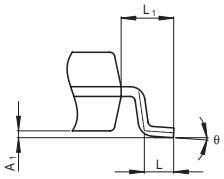




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	8.65	9.05
E	——	3.95	——
A 2	——	——	——
A 1	0.10	0.14	0.25
A	——	——	1.75
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	5.80	6.10	6.20
e	——	1.27	——
x	——	——	0.25
y	——	——	0.15
Z	——	——	0.635
L	0.40	0.60	1.27
L 1	——	1.08	——

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Colophon .3.0

HD74LS74A

Dual D-type Positive Edge-triggered Flip-Flops (with Preset and Clear)

REJ03D0415–0300
Rev.3.00
Jul.22.2005

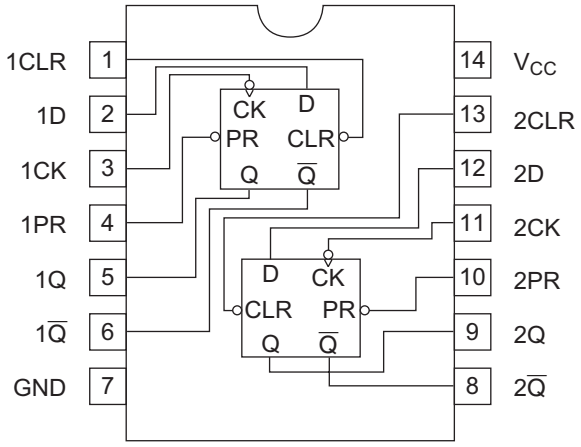
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS74AP	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS74AFPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LS74ARPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Function Table

Input				Output	
Preset	**Clear**	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H; high level, L; low level, X; irrelevant, ↑; transition from low to high level,
Q_0; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of $\overline{Q}_0$ or level of Q before the indicated steady-state input conditions were established.
*;This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Clock frequency		f_{clock}	0	—	25	MHz
Pulse width	Clock High	t_w	25	—	—	ns
	Clear Preset	t_w	25	—	—	
Setup time	“H” Data	t_{su}	20↑	—	—	ns
	“L” Data	t_{su}	20↑	—	—	
Hold time		t_h	5↑	—	—	ns

Note: ↑; The arrow indicates the rising edge.

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
		V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{IH} = 2 V
			—	—	0.4		I_{OL} = 4 mA
Input current	D	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	Clear		—	—	40		
	Preset		—	—	40		
	Clock		—	—	20		
	D	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Clear		—	—	–0.8		
	Preset		—	—	–0.8		
	Clock		—	—	–0.4		
	D	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Clear		—	—	0.2		
	Preset		—	—	0.2		
	Clock		—	—	0.1		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current		I_{CC}**	—	4	8	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IR}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

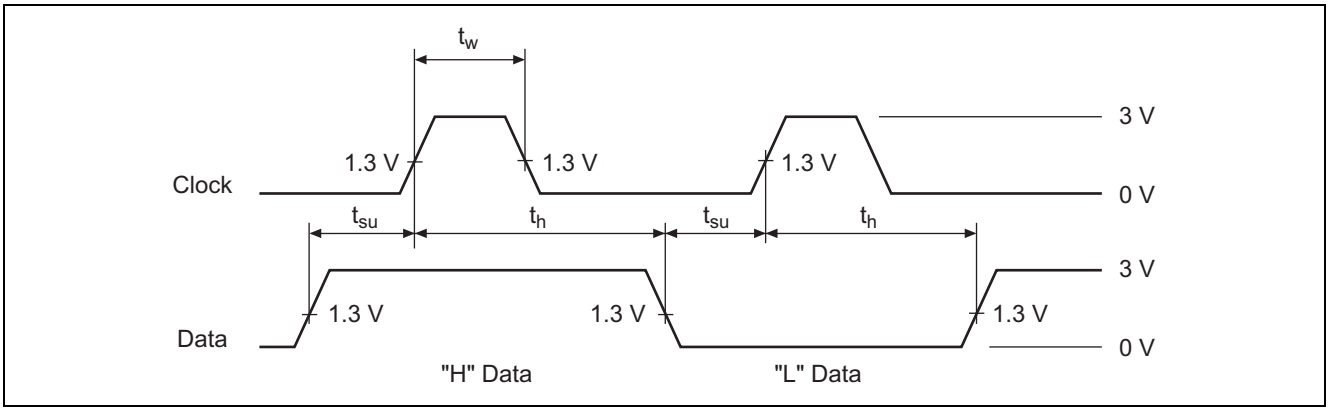
** With all output open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			25	33		MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clear, Clock or Preset	Q, $\overline{Q}$	—	13	25	ns	
	t_{PHL}			—	25	40	ns	

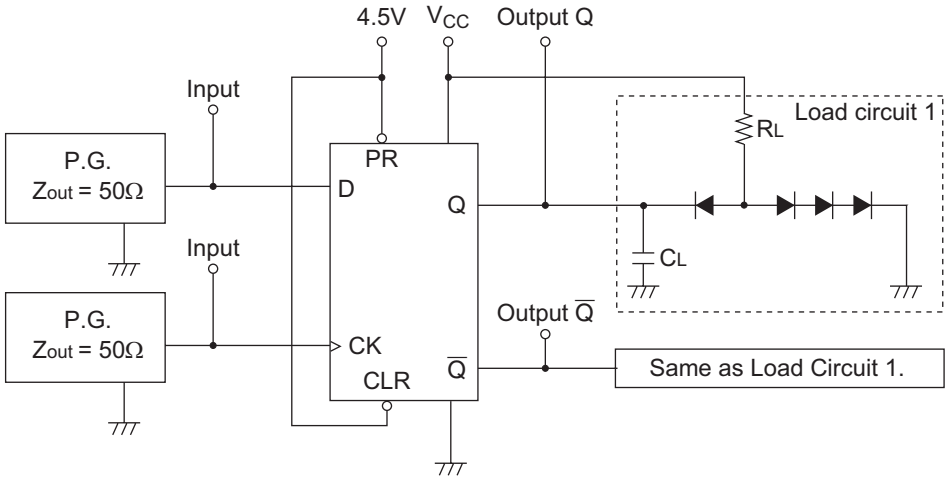
Timing Definition



Testing Method

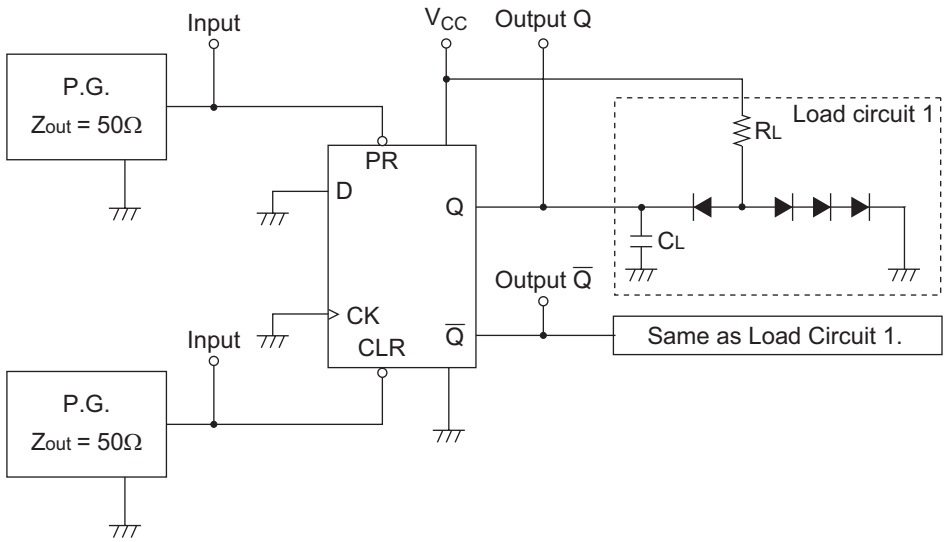
Test Circuit

1. f_{max}, t_{PLH}, t_{PHL} (Clock→Q, $\overline{Q}$)



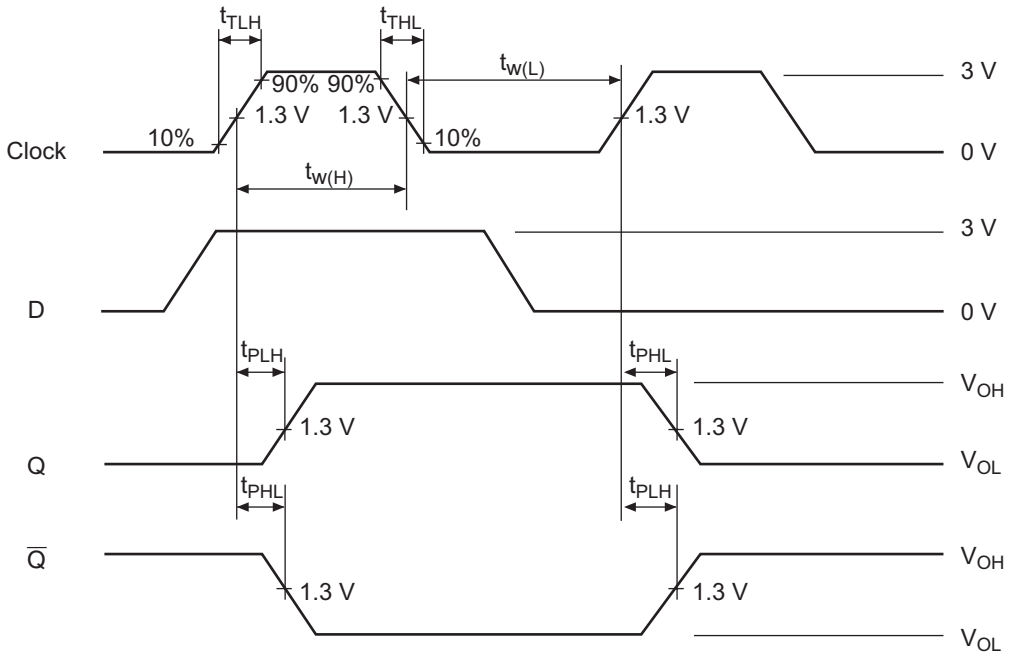
Notes:
1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

2. t_{PHL}, t_{PLH} (Clear or Preset→ Q, $\overline{Q}$)



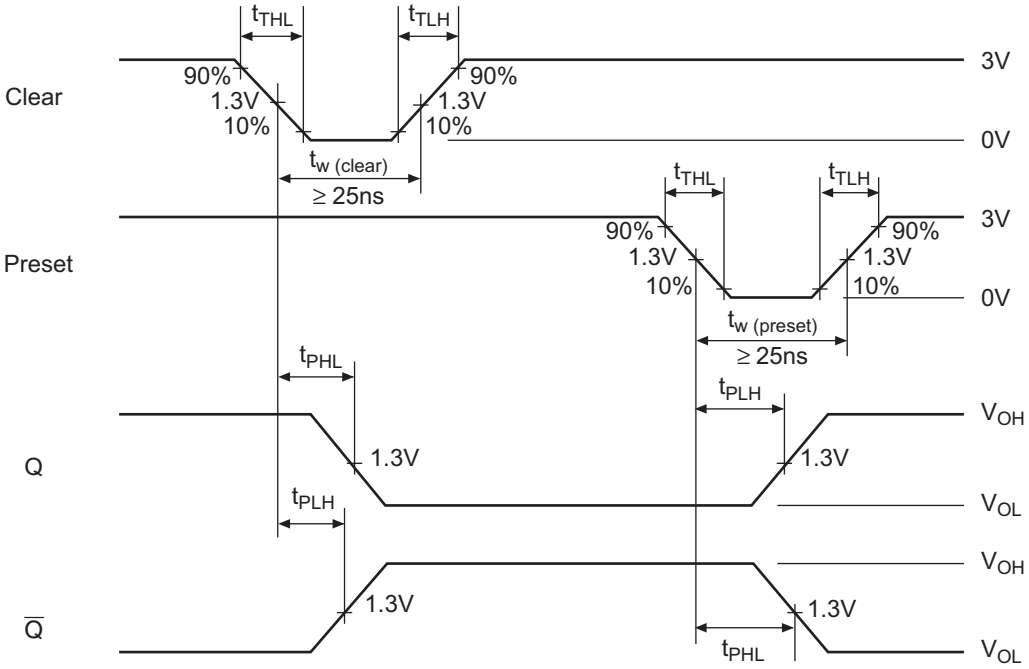
Notes:
1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

Waveforms 1



Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and for f_{max}, $t_{TLH} = t_{THL} \leq 2.5$ ns

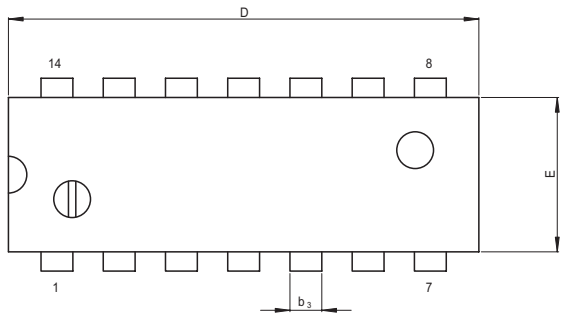
Waveforms 2

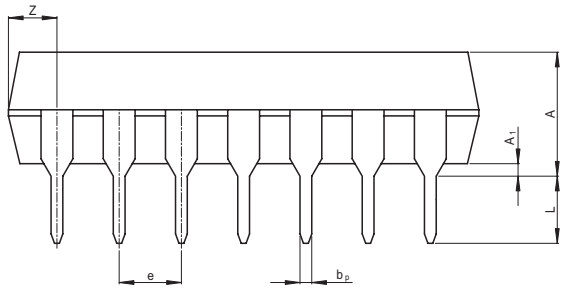


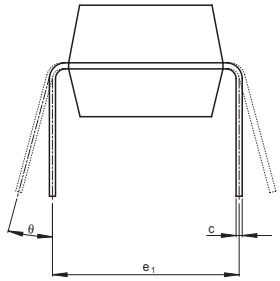
Note: Crear and presel input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz,

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-B	DP-14AV	0.97g



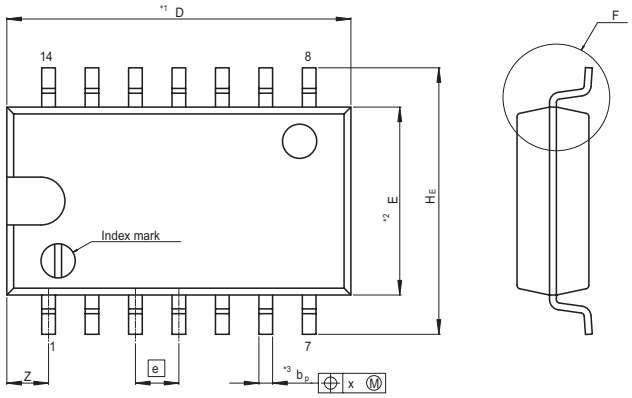


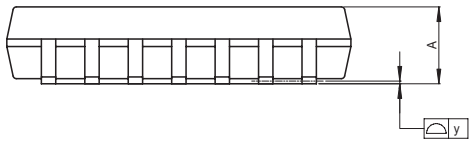


(Ni/Pd/Au plating)

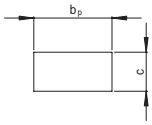
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A_1	0.51	——	——
b_p	0.40	0.48	0.56
b_3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	2.39
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g

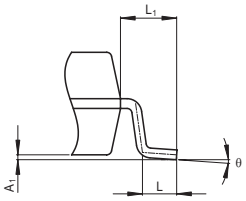




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



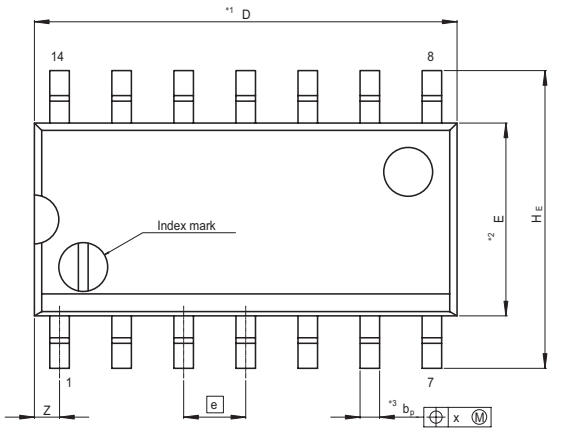
Terminal cross section
(Ni/Pd/Au plating)

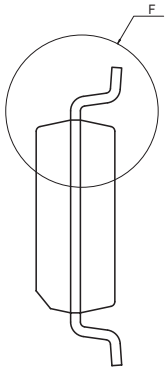


Detail F

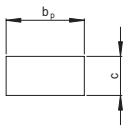
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	1.42
L	0.50	0.70	0.90
L_1	——	1.15	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-3.95x8.65-1.27	PRSP0014DE-A	FP-14DNV	0.13g

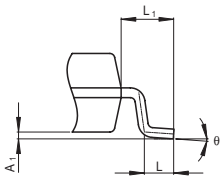




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.65	9.05
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L_1	—	1.08	—

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Colophon .3.0

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS75
Quad Latch

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is HIGH, and the Q output will follow the data input as long as the enable remains HIGH. When the enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go HIGH.

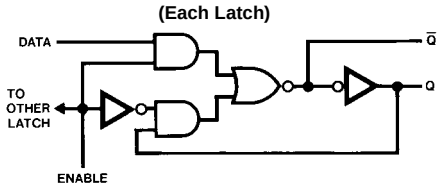
These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages.

Ordering Code:

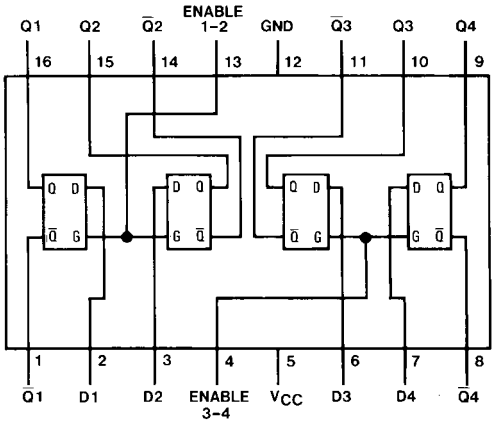
Order Number	Package Number	Package Description
DM74LS75M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS75N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Function Table (Each Latch)

Inputs		Outputs	
D	Enable	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = HIGH Level
L = LOW Level
X = Don't Care
Q_0 = The Level of Q Before the HIGH-to-LOW Transition of ENABLE

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
t_W	Enable Pulse Width (Note 5)	20			ns
t_{SU}	Setup Time (Note 5)	20			ns
t_H	Hold Time (Note 5)	0			ns
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.5		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	D			0.1	mA
			Enable			0.4	
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V	D			20	µA
			Enable			80	
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V	D			−0.4	mA
			Enable			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	12	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open and all inputs grounded.

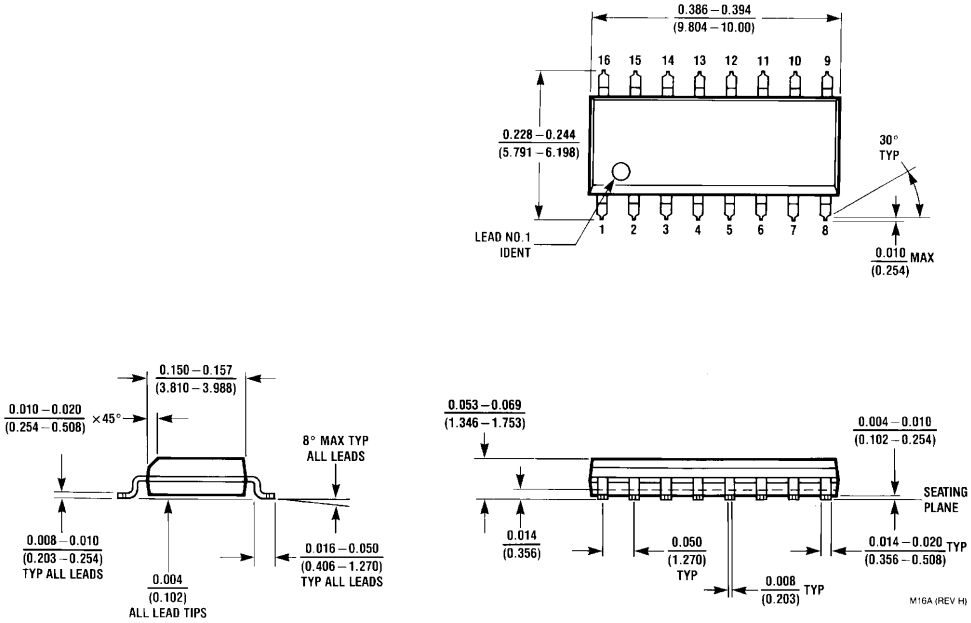
Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

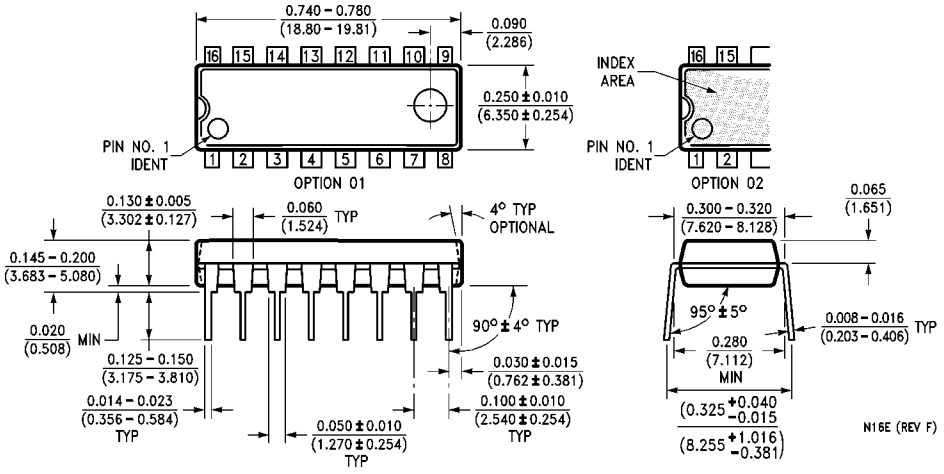
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	D to Q		27		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	D to Q		17		25	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	D to $\overline{Q}$		20		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	D to $\overline{Q}$		15		20	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Q		27		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Q		25		30	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to $\overline{Q}$		30		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to $\overline{Q}$		15		20	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS86
Quad 2-Input Exclusive-OR Gate

General Description

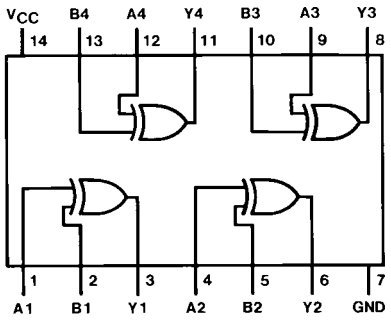
This device contains four independent gates each of which performs the logic exclusive-OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS86SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS86N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = A \oplus B = \overline{A}\,B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.2	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 4)		6.1	10	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 5)		9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CCH} is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

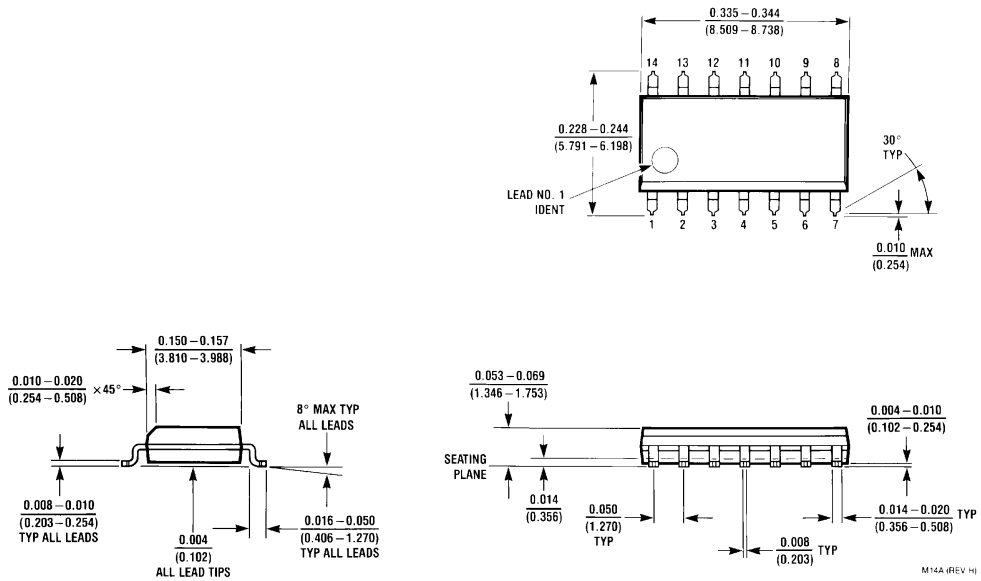
Note 5: I_{CCL} is measured with all outputs OPEN and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

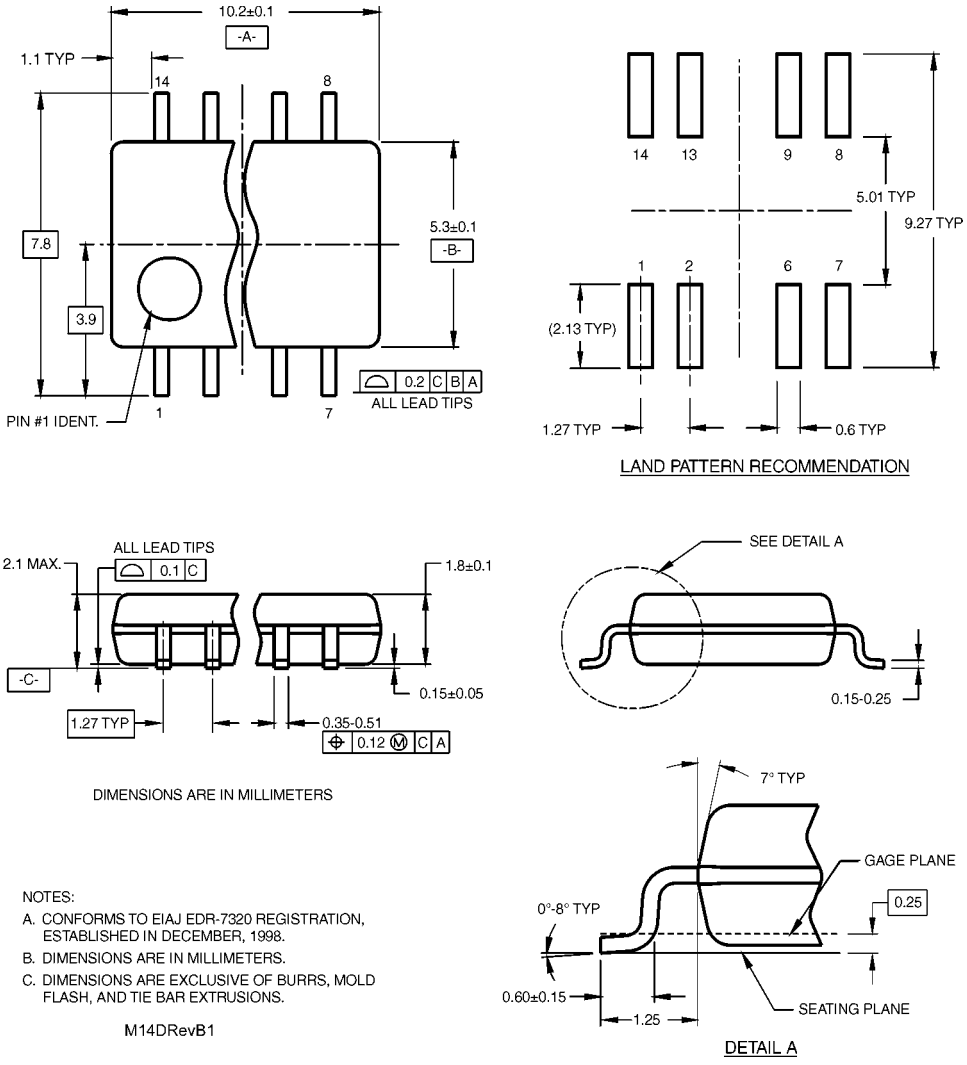
Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17		21	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			12		15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

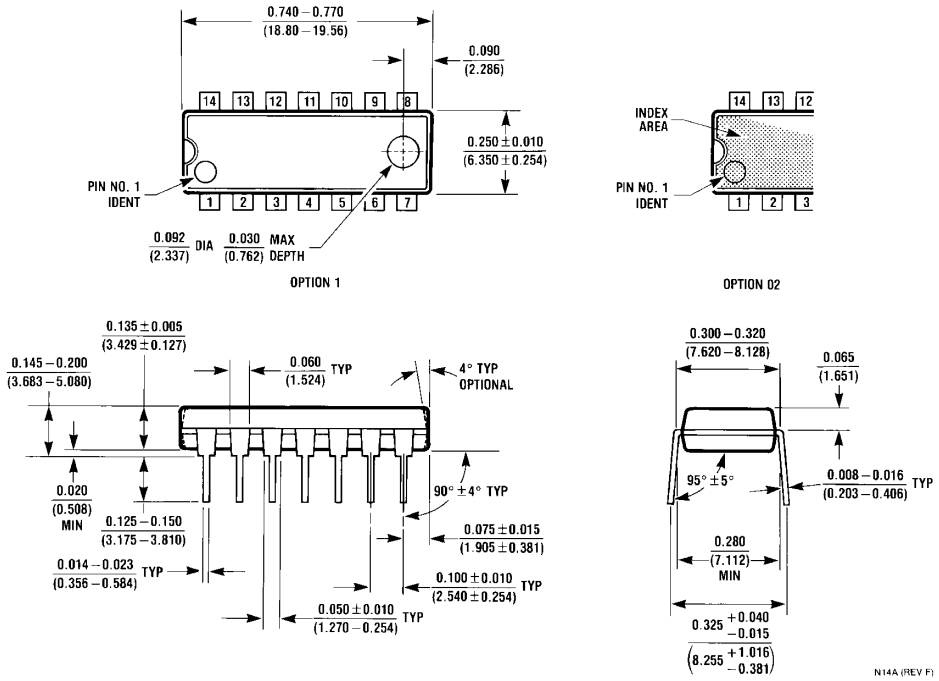
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

National Semiconductor

June 1989

DM74LS90/DM74LS93 Decade and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS90 and divide-by-eight for the 'LS93.

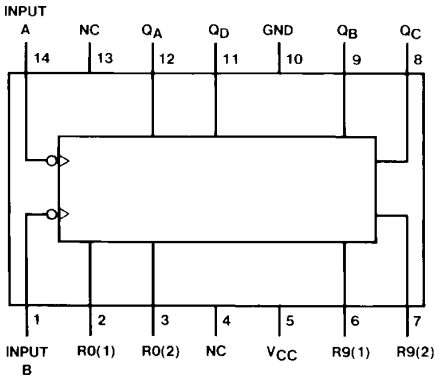
All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

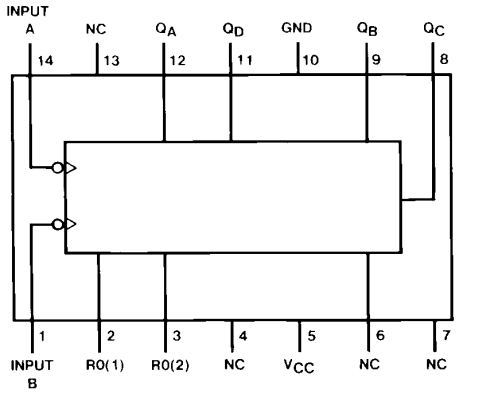
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagrams (Dual-In-Line Packages)



TL/F/6381–1

Order Number DM74LS90M or DM74LS90N
See NS Package Number M14A or N14A



TL/F/6381–2

Order Number DM74LS93M or DM74LS93N
See NS Package Number M14A or N14A

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage (Reset)	7V
Input Voltage (A or B)	5.5V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS90			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 1)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 2)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 1)		25			ns
t_{REL}	Reset Release Time (Note 2)		35			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 1: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = Min$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = Min$, $I_{OH} = Max$ $V_{IL} = Max$, $V_{IH} = Min$		2.7	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = Min$, $I_{OL} = Max$ $V_{IL} = Max$, $V_{IH} = Min$ (Note 4)			0.35	0.5	V
		$I_{OL} = 4$ mA, $V_{CC} = Min$			0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = Max$, $V_I = 7V$	Reset			0.1	mA
		$V_{CC} = Max$ $V_I = 5.5V$	A			0.2	
			B			0.4	

’LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

’LS90 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		52	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Recommended Operating Conditions

Symbol	Parameter		DM74LS93			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	
		B to Q_B	0		10	
t_W	Pulse Width (Note 1)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 2)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 1)		25			ns
t_{REL}	Reset Release Time (Note 2)		35			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	

'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'LS93 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		85	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		90	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Function Tables

LS90
BCD Count Sequence
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS90
Bi-Quinary (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LS93
Count Sequence
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LS90
Reset/Count Truth Table

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

LS93
Reset/Count Truth Table

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B for BCD count.

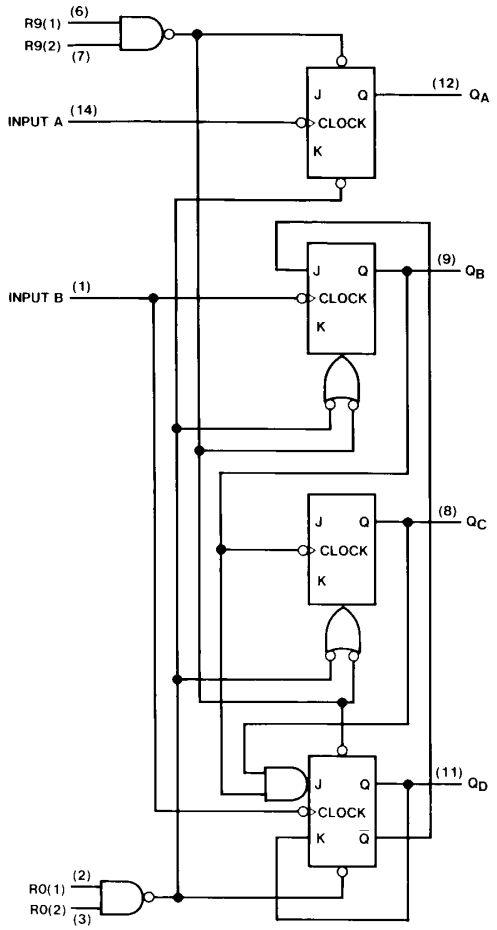
Note B: Output Q_D is connected to input A for bi-quinary count.

Note C: Output Q_A is connected to input B.

Note D: H = High Level, L = Low Level, X = Don't Care.

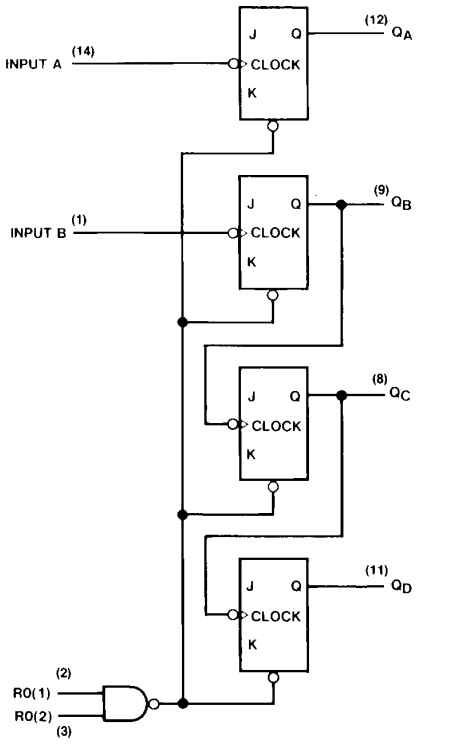
Logic Diagrams

LS90



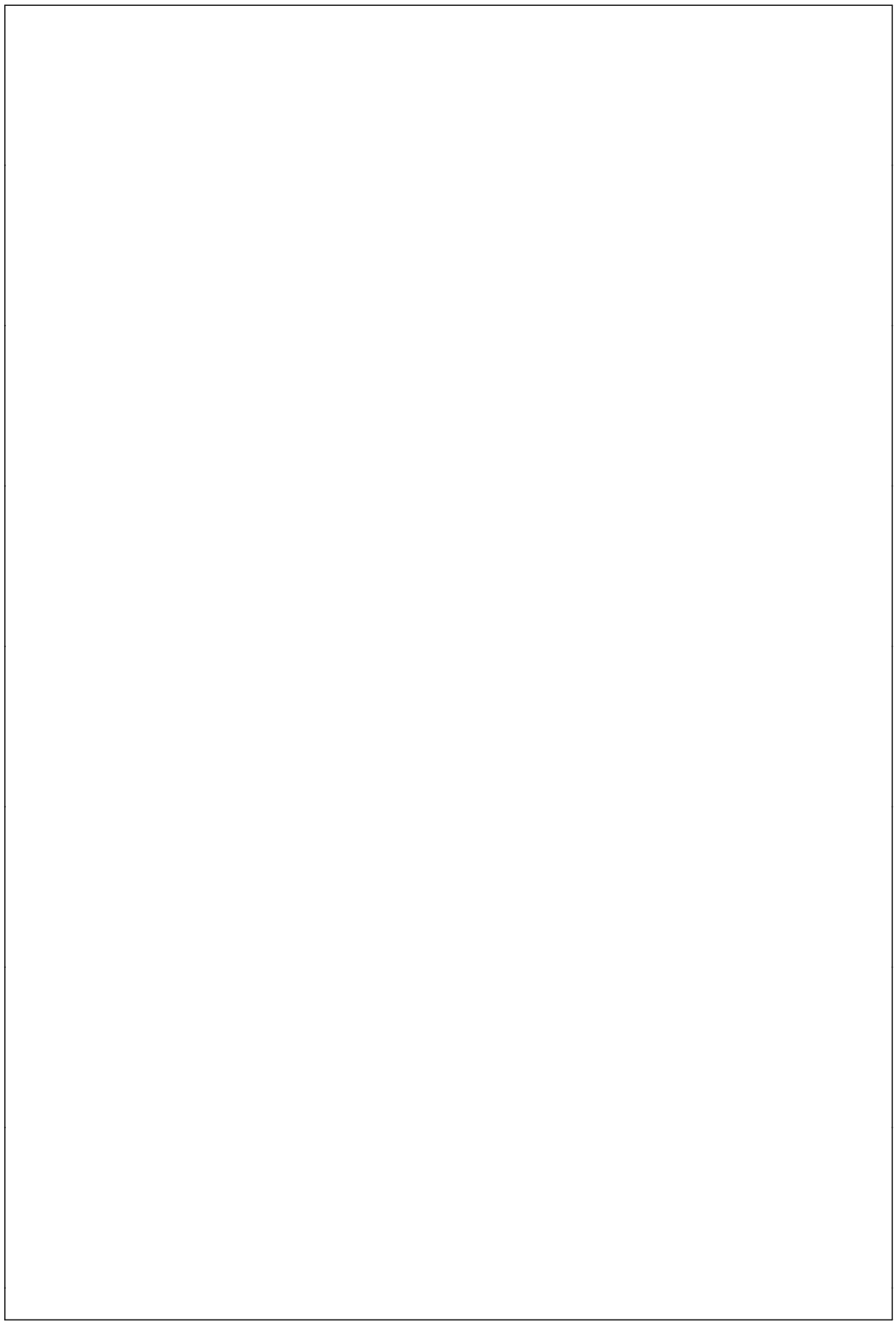
TL/F/6381–3

LS93

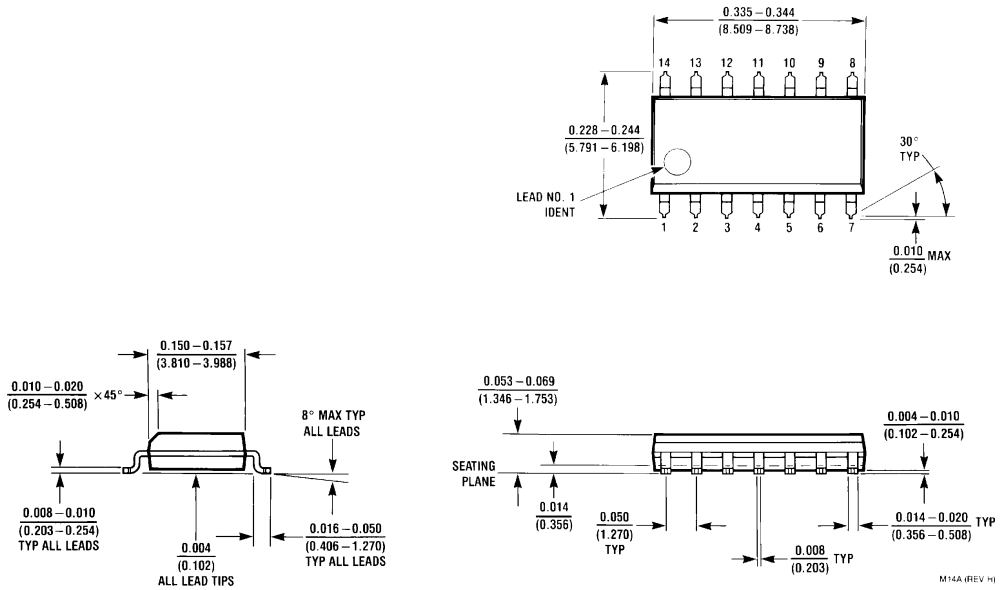


TL/F/6381–4

The J and K inputs shown without connection are for reference only and are functionally at a high level.

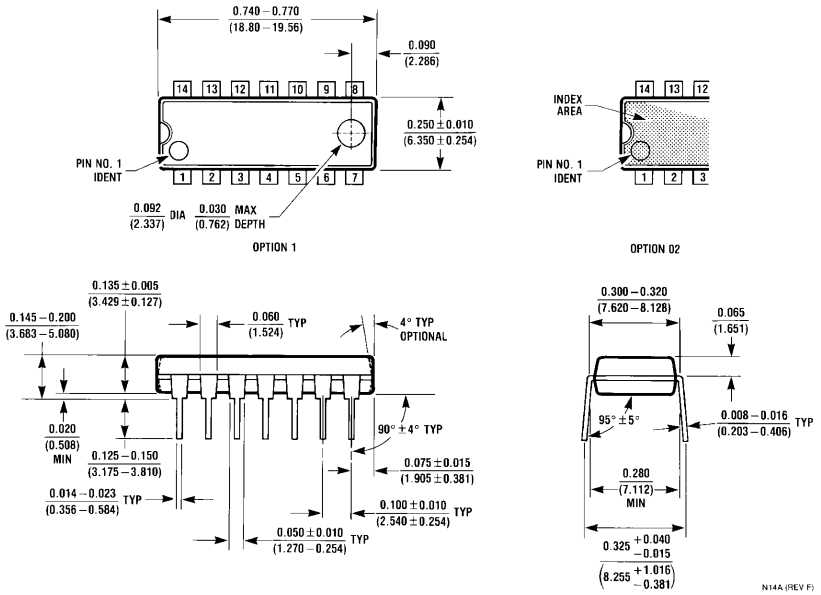


Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS90M or DM74LS93M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS90N or DM74LS93N
NS Package Number N14A

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0.56 Inch Red Single Digit Display
OSL10561-IRA
Common Anode type

■ Features

- High luminous LEDs
- Long lifetime operation
- IC compatible
- Low power dissipation
- Black surface & white segment or dot

■ Applications

- Counting device
- Clock

■ Photo

■ Absolute Maximum Rating (Ta=25℃)

Item	Symbol	Value	Unit
DC Forward Current	I_F	20	mA
Pulse Forward Current*	I_{FP}	100	mA
Reverse Voltage	V_R	5	V
Power Dissipation	P_t	40	mW
Operating Temperature	Topr	-30 ~ +70	℃
Storage Temperature	Tstg	-40~ +85	℃
Lead Soldering Temperature(1.6mm from seating plane)	Tsol	260℃/5sec	℃

■ Electrical -Optical Characteristics (Ta=25℃)

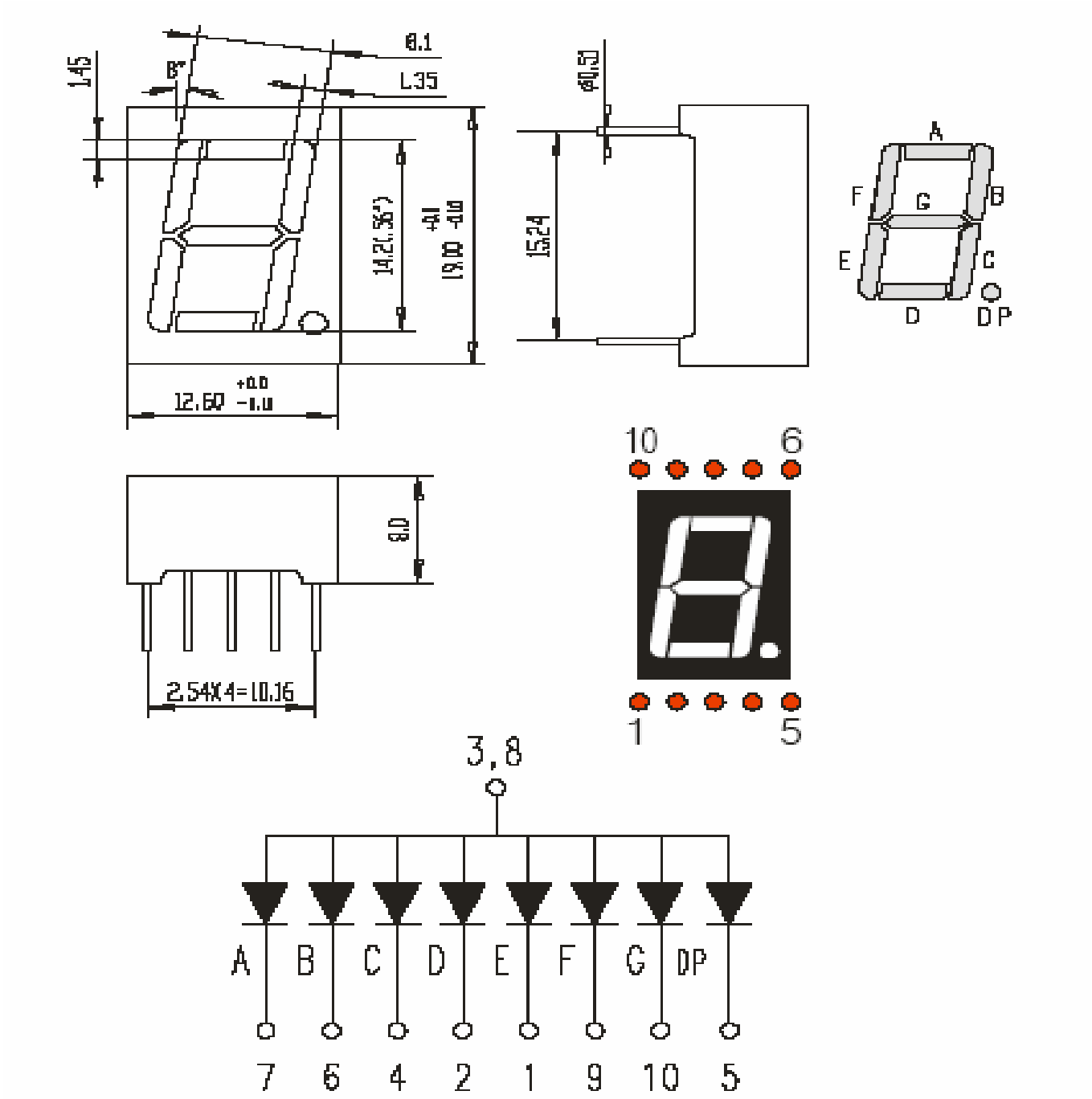
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Forward Voltage	V_F	I_F=20mA	-	2.1	2.5	V
DC Reverse Current	I_R	V_R=5V	-	-	20	μA
Domi. Wavelength*	λ_D	I_F=20mA	-	625	-	nm
Luminous Intensity*	Iv	I_F=20mA	-	90	-	mcd

***1 Tolerance of dominant wavelength is±1nm**

***2 Tolerance of luminous intensity is±15%**

0.56 Inch Red Single Digit Display
OSL10561-IRA
Common Anode type

■ **Package dimensions and pin function**



管脚顺序：从数码管的正面观看,见图。

图中所有尺寸单位为 mm；未标注误差范围的尺寸误差范围为±0.25mm。

0.56 Inch Blue Single Digit Display
OSL10561-LB
Common Cathode type

■ Features

- High luminous LEDs
- Long lifetime operation
- IC compatible
- Low power dissipation
- Black surface & white segment or dot

■ Applications

- Counting device
- Clock

■ Photo

■ Absolute Maximum Rating (Ta=25℃)

Item	Symbol	Value	Unit
DC Forward Current	I_F	20	mA
Pulse Forward Current*	I_{FP}	100	mA
Reverse Voltage	V_R	5	V
Power Dissipation	P_t	66	mW
Operating Temperature	Topr	-30 ~ +70	℃
Storage Temperature	Tstg	-40~ +85	℃
Lead Soldering Temperature(1.6mm from seating plane)	Tsol	260℃/5sec	℃

■ Electrical -Optical Characteristics (Ta=25℃)

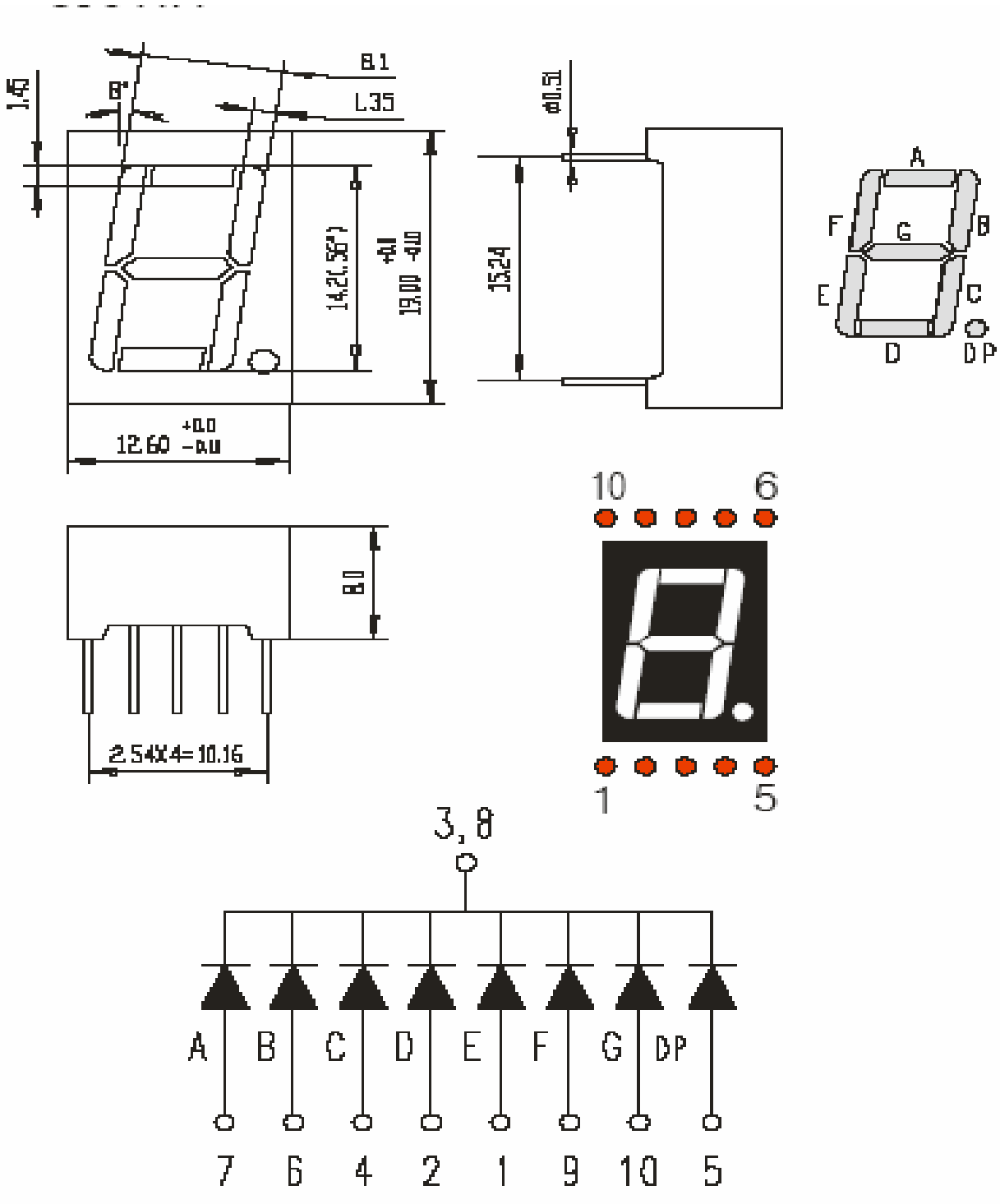
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Forward Voltage	V_F	I_F=20mA	-	3.3	4.0	V
DC Reverse Current	I_R	V_R=5V	-	-	20	μA
Domi. Wavelength*	λ_D	I_F=20mA	-	470	-	nm
Luminous Intensity*	Iv	I_F=20mA	-	50	-	mcd

***1 Tolerance of dominant wavelength is±1nm**

***2 Tolerance of luminous intensity is±15%**

0.56 Inch Blue Single Digit Display
OSL10561-LB
Common Cathode type

■ **Package dimensions and pin function**



管脚顺序：从数码管的正面观看,见图。

图中所有尺寸单位为 mm；未标注误差范围的尺寸误差范围为±0.25mm。